A Survey of Optical and Electronic Delay Lines with a Case Study on Using Optical Delay Lines in 65 nm CMOS Optical Receivers

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***Abstract*—This paper presents a survey of electronic delay lines and recent advances in silicon photonics-based optical delay lines targeting data and clock synchronization in the optical receiver. Important considerations such as delay range, delay resolution, tunability, and power consumption are discussed. Measurements of two optical receivers developed in CMOS 65 nm utilizing silicon photonic based delay lines are presented demonstrating the benefits of optical delays. Superior energy efficiency of 156 fJ/bit is achieved at 17 Gb/s.**

Keywords—Delay lines, optical delay line, silicon photonics, high data rates, demultiplexing.

I. Introduction

Recently there has been an increased interest in the co-design of electronics and photonics to improve the performance of optical receivers and reduce cost. There are several examples of this in the literature [1–6]. This includes relocating passive components from the electronic side to the photonic side [1,2] reducing the area, and thus, the fabrication cost of the electronic chip. In [3], the connection between a photodiode and the transimpedance amplifier is optimized allowing the receiver to achieve superior sensitivity. More recently, the receivers reported in [4–6] attempted to exploit silicon photonics (SiP) delay lines to do spatial processing of data enabling the removal of clock generation circuits in the receiver. This resulted in low-complexity high-speed optical receivers with superior energy efficiency. The recent emergence and development of silicon-based optical delay lines that are suitable for integration with electronic ICs may lead to replacing some of the electronic delay lines with their optical counterpart [5–6].

In this paper, several CMOS and optical delay lines are reviewed and compared in terms of resolution, delay range, power consumption, and tunability. Two optical receivers exploiting optical delay are presented as well demonstrating that high energy efficiency and low-complexity receivers can be designed. Section II describes some of the most used electronic delay lines. Section III describes recent developments of optical delay lines. Section IV briefly addresses some of the considerations for selecting the optimum delay line for a given application. Section V presents two receivers exploiting optical delay lines. Finally, section VI concludes the work.

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II. CMOS Delay Lines

Electronic delay lines are the most commonly used due to their low complexity and low cost. These delay lines can have a single output or can have multiple outputs where the output of the required delay is selected. Delay line elements can be tuned with an analog signal or can be digitally controlled. We review four different delay line architectures.

A. Inverter-based tapped delay line and single output delay line architectures

In the inverter-based tapped delay line architecture [7], delay line elements are cascaded and the output corresponding to the required delay is selected. The most commonly used delay element is an inverter, but other delay elements such as flip-flops [8] can be used as well. This architecture is shown in Fig. 1(a). A mux is needed to select the required delay. Alternatively, the single output implementation is shown in Fig. 1(b) and could be used to eliminate the multiplexer. This delay line is digitally controlled using tri-state inverters that are enabled and disable based on the required delay.

These architectures can have a wide delay range and the range increases with the number of stages, but the resolution is limited to one or two gate delays of the delay element. Since the resolution is set by the gate delay, it improves with the technology node where smaller nodes allow for finer resolutions. The power consumption of this type of delay line is high and increases with delay range as more delay elements are needed. The two lines can only be used with digital signals.

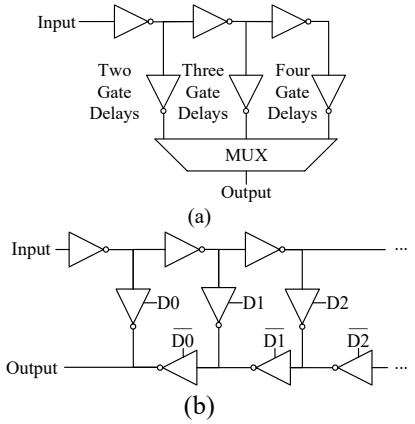


Fig. 1. (a) Inverter-based tapped delay line. (b) Single output delay line.

B. Sub-gate resolution two-path delay line

The architecture in Fig. 2 allows for sub-gate delays. In this architecture [9], the digital input signal is fed to two different paths with a different delay (fast path and slow path). MOS capacitors are used to slow the signal in the lower slow path. The difference between the two paths is less than a gate delay and hence a sub-gate delay is achieved. The control signal is used to enable the appropriate path based on the required delay. The range of this technique is limited, and the power consumption is higher than the previous architectures discussed for a given range. This delay line does not scale linearly.

C. Analog delay buffer based delay lines

A delay line element that can be used to build analog delay lines is the analog buffer shown in Fig. 3 [10]. This delay line is controlled by an analog signal and the delay is adjusted by varying the control voltages V_C and V_{CB} which in turn changes the load of the circuit changing the speed of the buffer. Analog buffer-based delay lines can have a good resolution but are power-hungry due to static power consumption.

D. Supply voltage controlled and current starved delay lines

In these types of delay lines, either the supply voltage is used to control the delay of the delay line (Fig. 4(a)) using an analog signal [11], or the biasing current is changed using a digital signal (Fig. 4(b)) [12]. In either case, the current drawn is changed and the rate at which the load capacitor is charged changes accordingly. The first technique requires a supply source capable of providing substantial amounts of current and the resulting delay is not as fine as other techniques. The second technique is reported to achieve good resolution (2 ps) and range (320 ps) [12]. The work in [13] provides a more comprehensive discussion of various electronic delay lines.

III. Optical Delay Lines

Optical delay lines can be divided into mechanically controlled, passive, and electronically controlled delay lines.

A. Mechanically controlled free space delay lines

In this kind of optical delay lines, a gap opening is controlled mechanically changing the distance the light must traverse and thus controlling the delay. Products of these delay lines are readily available (e.g. ODL-330) and can have delay ranges of 400 ps. The resolution is mechanically controlled and can be as small as 0.2 ps. As these delay lines are passive, they consume no power. Free space delay lines can attenuate the signal and have an insertion loss in the order of 1.5 dB. While these delay lines have an impressive resolution, range, and do not consume power, they are not suitable for integrated systems due to their gap size (e.g., 45 mm in ODL-330) and the mechanical control.

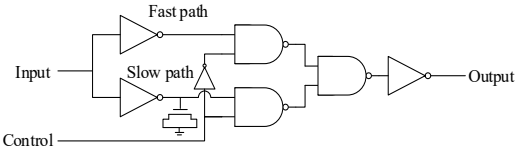


Fig. 2. Two path delay line capable of sub-gate delays.

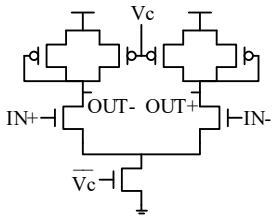


Fig. 3. Analog buffer that can be used to delay analog signals and controlled through adjusting the load.

B. Passive integrated optical lines

This delay line is implemented using an optical waveguide of a certain length corresponding to a fixed required delay. This delay line can be implemented on-chip and is suitable for integration with electronic receivers and systems. These delay lines can have a small size with a compact layout depending on the required delay. For example, in [4] for a 100 ps delay line of 7.2 mm in length, the rectangular nested layout has a size of 250 μm × 250 μm. This delay line has low insertion loss as well which can be as low as 0.2 dB for 50 ps delay. Since these delay lines are passive, they consume no power. These delay lines are not tunable but can have accurate delays. An error of 3 ps can be expected for a 50 ps delay [4]. In section V, we review two optical receivers that take advantage of such optical delay lines. A detailed description of these delay lines is provided in [4].

C. Electronically controlled optical delay lines

Integrated optical tunable delay lines can be made tunable by using ring resonators and Mach–Zehnder interferometers (MZIs). One such implementation is reported in [14] and is shown in Fig. 5. In this implementation, a ring resonator is used to fine control the delay and can have a continuous delay range of up to 23 ps. The MZI array of eight elements is used as a coarse delay where they are used to select the delay path. This technique is reported to allow for a continuous delay of up to 1.27 ns. The power consumption is 12–33 mW depending on the delay. This line has a high insertion loss of 12.4 dB.

IV. Trade-Off Considerations

When selecting the appropriate delay line, the requirements of the application need to be considered. Considerations include

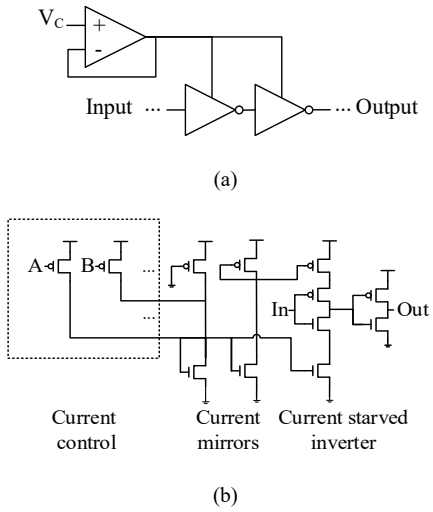


Fig. 4. (a) Supply controlled delay line. (b) Current starved delay line.

power consumption, resolution, range, tunability, tuning mechanism and signal, integrability, and type of input signal (electrical, optical, analog, digital). All electronic delay lines reviewed can be used exclusively with digital signals, except for the analog buffer. Moreover, cascading analog buffers to increase the range limits the bandwidth of the chain making this type of delay lines only suitable for slow analog signals or short delays. Optical delay lines have no limitation on the type of information the optical signal carries, digital or analog.

As discussed in the previous section, electronic delay lines exhibit a trade-off between delay range and power consumption. Higher delays and wider delay range usually result in higher power consumption. Free space and passive integrated optical delay lines do not suffer from this limitation and consume no power regardless of the delay or the range. This trade-off is still true for electronically controlled optical delay lines.

The resolution of electronic delay lines depends on the technique used. Resolutions down to 1 ps can be achieved. However, mechanically and electronically tunable optical delay lines offer superior performance in this regard. Mechanically tunable delay lines have a resolution as small as 0.2 ps and electronically tunable optical delay lines offer continuous delay. Passive integrated optical delay lines are not tunable.

In terms of integration, electronic delay lines are simpler and suitable for digital systems and slow analog signals but can be limited in terms of resolution and bandwidth. Optical delay lines are more difficult to integrate as they need to be implemented on a different technology node such as silicon photonics and are also more difficult to control as they need external mechanical or electronic tuning. However, they could provide virtually infinite bandwidth, infinitesimal resolution, or zero power consumption.

V. Passive Optical Delay Lines to Replace Clock Generation Circuits in the Optical Receiver

We have developed two receivers [5–6] that leverage passive integrated optical lines to replace clock phase generation blocks in sub-rate sampling optical receivers. We use those examples to demonstrate the benefits of employing delay lines.

In conventional sub-rate sampling receivers, four (Fig. 6(a)) or two clock phases (Fig. 6(b)) are generated to sample incoming bits. This is done to relax the regeneration time of the latches in the receivers. The sum of the sample phase, the hold phase, and the regeneration phase times is thus four unit intervals and two unit intervals for two and four clock phases, respectively. It was found that a significant portion of the power consumption of the receiver is due to clocking [5]. This motivated the development of a co-designed optical receiver using passive optical delay lines to replace those clocking circuits with optical delay lines and splitters that are used to delay the input signal allowing the receivers to operate using only one clock phase. This is demonstrated for a demux-by-four system in Fig. 6(c) and for a demux-by-two in Fig. 6(d).

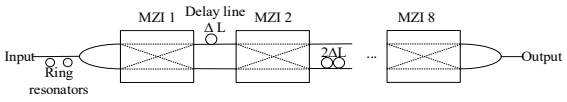


Fig. 5. Electronically tunable optical delay lines.

The optical passive structure, shown in Fig. 7 [4] for a demux-by-four system, consists of a grating coupler (GC) followed by an optical splitter that divides the signal by four and by two four optical lines each used to delay the signal by one bit relative to the previous bit, with the first output having no delay. The optical outputs are fed to a photodetector (PD) for detection.

The coupling ratio of the directional couplers is adjusted such that the output power is the same for each of the four outputs considering the insertion loss of the delay lines. Four variants of the delay lines were designed at 10 Gb/s and 20 Gb/s. The two variants at 10 Gb/s have lengths of 7.2 mm and 8.2 mm for cross-sections of 220 nm × 500 nm and 220 nm × 3 μm with 3.2 dB and 0.3 dB insertion loss, respectively. The two variants at 20 Gb/s have lengths of 3.6 mm and 4.1 mm for cross-sections of 220 nm × 500 nm and 220 nm × 3 μm with 1.5 dB and 0.1 dB insertion loss, respectively. These delays are fixed but are suitable for the intended application of a fixed speed receiver.

The first receiver, detailed in [5], is a demux-by-four system shown in Fig. 8(a) and consists of four sub receivers [5]. Each sub receiver consists of a common gate transimpedance amplifier used to convert the photocurrent into voltage, followed by two cascode voltage gain stages with inductive peaking. A current-mode logic (CML) latch is used to convert the input signal into a return-to-zero digital signal. A pseudo-NMOS inverter is used to boost the voltage level followed by a D flip-flop to convert the pattern into a non-return-to-zero form. This

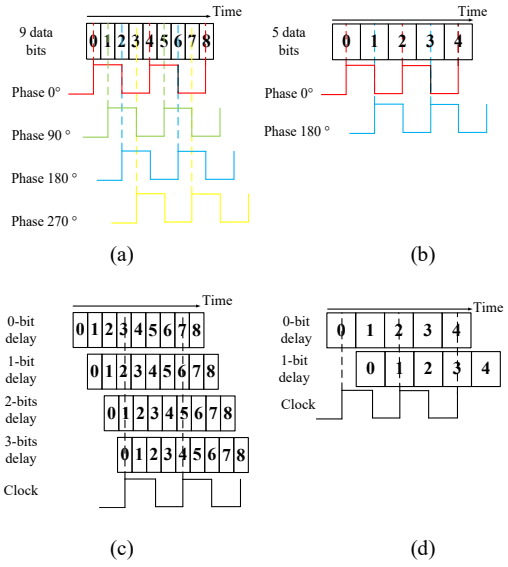


Fig. 6. (a) Sampling in the conventional demux-by-four receiver. (b) Sampling in the conventional demux-by-two receiver. (c) Sampling in the proposed demux-by-four and (d) demux-by-two receivers.

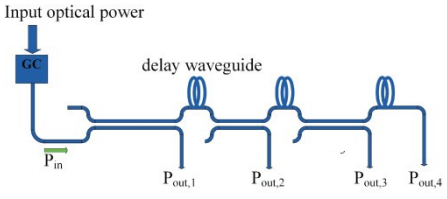
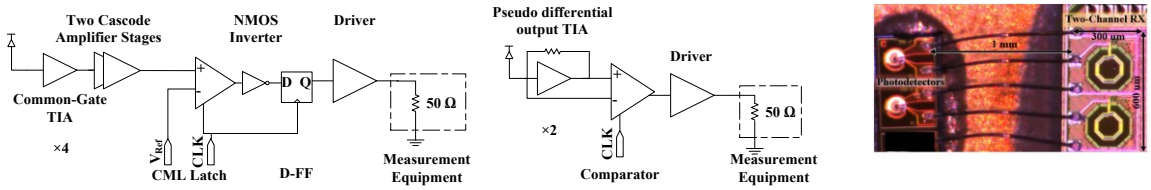


Fig.7. Optical split-delay structure. [4]



(a) (b) (c)

Fig. 8. (a) The demux-by-four receiver with quarter-rate output. (b) Demux-by-two receiver with a half-rate output based. (c) A micrograph of the demux-by-two receiver showing the connection between the photodetectors and the TIA [6].

receiver was measured at 12.5 Gb/s and achieved an energy efficiency of 1.93 pJ/bit. Only 10% of the power consumption is due to clocking. This is an improvement over the 30% to 45% reported in state-of-the-art receivers. This technique also removes the need for accurate quadrature and duty cycle detection and correction circuits used to ensure that clock phases are properly aligned and have the correct duty cycle. This further reduces complexity. The downside of this technique is the insertion loss of the optical splitter that degrades the sensitivity by 6 dB. The measured sensitivity is -4 dBm at a bit error rate (BER) of 10^{-12}. In this receiver, the photodetector is external and connected to the chip using an SMA cable. The chip is wire bonded to the printed circuit board through a package.

Similarly, a demux-by-two receiver, detailed in [6], was also developed and is shown in Fig. 8(b). This optical receiver consists of two sub receivers. Each sub receiver consists of a high-bandwidth gain-improved transimpedance amplifier with a pseudo-differential-output followed by a comparator with offset nulling. In this receiver, the photodetector is wire bonded to the chip and in both receivers, mechanical delay lines are used and are tuned manually for this proof-of-concept, but passive optical delay lines could be used as well. The simplified clocking scheme and the use of a single gain stage allowed this receiver to achieve a superior energy efficiency of 156 fJ/bit at 17 Gb/s. To the best authors' knowledge, this is the most energy efficiency optical receiver reported to date. The insertion loss of the splitter is only 3 dB compared to 6 dB in the previous design improving the sensitivity. The measured sensitivity is -7 dBm BER of 10^{-12}. A micrograph of this chip is shown in Fig. 8(c). The implementations of both receivers are detailed in [5,6]. A performance summary is shown in Table I.

TABLE I
THE PROPOSED RECEIVERS PERFORMANCE SUMMARY

Spec	[5]	[6]
Speed	12.5 Gb/s	17 Gb/s
Sensitvity at BER = 10^{-12}	-4 dBm	-7.5 dBm
Optical split loss	6 dB	3 dB
Energy efficincy	1.93 pJ/bit	0.156 pJ/bit

VI. Conclusion

Commonly used electronic delay lines are reviewed and compared with optical delay lines. It was found that in some cases optical delay lines can offer higher resolution and potentially lower power consumption. However, they are difficult to integrate. Optical delay lines can lead to improved designs. Two recently developed optical receivers leveraging optical delay lines are discussed to showcase the benefits of employing optical delay lines. In those, superior energy efficiency is achieved due to clock generation circuits removal.

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