Low power mm-wave transmitter architecture with on-chip resonator/All digital Phase Locked Loop (PLL)

By

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Abstract

Wireless sensor networks have been a research subject in many disciplines. The common building block to all wireless sensor nodes is the wireless transceiver. As lower frequencies, such as the 2.4GHz ISM band, became congested, a need for low power, small size and self-contained (i.e. with no external components) transceivers has become apparent. To address this, a primary focus of this thesis is the design of the transmitter part of the transceiver.

The first topic of this thesis is a system level analysis. This system analysis investigates the impact of the form factor of wireless sensor nodes on the optimal RF frequency. The criterion for optimality is selected as the energy efficiency of the entire system including the transmitter and receiver. The conclusion of this analysis supports the choice of 60GHz as the desired frequency for the design of the transmitter.

As a second topic of the thesis, two novel ultra-low power (ULP) transmitters are proposed, and the designs are presented. Both transmitters are unconventional in the sense that they have no power amplifiers and Phase-locked loops (PLL) involved. The lack of external crystals is compensated by the existence of an on-chip resonator at the Tx side and a frequency agnostic receiver type. The power amplifier is eliminated by having a switched oscillator driving directly the antenna. The two versions of the transmitters were designed in 65nm CMOS technology from GF. One consumed 3.3mW of power while delivering -2dBm of power to the output, while the other consumed 5mW of power while delivering 2dBm of power to the output.

A third topic of this thesis is the design of a novel all-digital phase-locked loop (DPLL) which can be used in the transmitter to synchronize the data and the oscillator clock. The design can be modified and used as a clock and data recovery on the receiver side. The proposed DPLL can be used as a frequency demodulator without any changes

to the original architecture. The DPLL was simulated using 65nm CMOS. An operating range of one decade was achieved (20MHz-220MHz) while consuming a power of less than 100uW.

This research was supported by the Government of Abu Dhabi to help fulfill the vision of the late President Sheikh Zayed Bin Sultan Al Nayhan for sustainable development and empowerment of the UAE and humankind.

Acknowledgments

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Needless to say, I am very thankful to my family, my friends and my colleagues who have been extremely supportive of me during my time here at Masdar.

Last but not least, I am very grateful to Masdar Institute of Science and Technology and Semiconductor Research Corporation (SRC) for funding my education and this project.

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CHAPTER 1

Introduction

1.1 Background

Within the context of wireless sensor networks (WSN), mm-wave frequencies promise the advantage of very small antennas and hence a small form factor for the sensor node. For applications with severely constrained form factors, mm-wave frequencies are perhaps the only option as systems operating in the microwave range (300MHz-3GHz) require antennas that are centimeters in size. If this size was smaller, then the radiation efficiency degrades significantly. Millimeter wave operating frequencies, on the other hand, would render antenna sizes of less than 1mm in length. An energy advantage may emerge compared to microwave frequency systems, and that is one of the subjects presented in this work. A mm-wave transceiver is needed for WSN and will require the rethinking of architectures and circuits currently in use for high data rate applications already defined by 802.5.11 IEEE standard. Wireless sensor network applications demand extreme energy efficiency. This is a daunting task at mm-waves due to the high-frequency carrier.

For WSN applications with a constrained form factor, it is essential to develop an ultra-low power transmitter and receiver for the sensor node to sustain long operation time. Consequently, many building blocks, which may be thought of as necessary building blocks for state-of-art transceivers, need to be eliminated to satisfy the requirement of low average power and peak instantaneous power. Low average power

opens up the possibility of energy harvesting whereas a reduced peak instantaneous power opens up the possibility of using a flexible battery with small volume. Blocks such as the Low Noise Amplifier (LNA), PLL's, and the Power Amplifier (PA) contribute a significant portion to the total power consumption of the system. These blocks can be eliminated, reducing the maximum distance allowed between the transmitter and the receiver or, equivalently, the sensitivity of the receiver. This reduction in distance is acceptable in short distance communication systems, the target application for the design proposed in the thesis.

Therefore, it is important to develop a minimalist transceiver approach for those WSN applications. On the transmitter side, a minimalist architecture can be achieved by developing a 60GHz type oscillator. Its current can be switched on and off according to a data stream. The oscillator drives directly a 50Ω load antenna or the measurement instrument port input impedance. Hence, one of the targets of this research is to develop an On-Off Keying (OOK) transmitter consisting of a data switched oscillator driving a 50Ω load.

Moreover, this research investigates the optimal frequency of operation of systems with constrained for factor. On one hand, lower frequencies can result in large form factor and higher power consumption due to frequency accuracy (need PLL). On the other hand, higher frequencies render smaller antenna sizes but have higher attenuation as predicted from Friss transmission formula [1]. Therefore, it is important to choose the dimensions of the antenna and the optimal operating frequency appropriately according to a specified form factor.

Another important building block of communication systems is the Phase Locked Loop (PLL) which can be used in conjunction with an oscillator to generate the On-Off Keying (OOK) data. For some applications where frequency accuracy is paramount, a

PLL is required. As an ultra-low power system is required, the PLL power consumption should be as low as possible. In addition, a very short pull-in time is required. This will reduce the transient power consumption. An analog PLL will have a better jitter performance, but a digital PLL have smaller form factor (No external loop filter capacitors) and can be ported from one technology node to another without extra design effort. Besides, in some situations, an all-digital PLL can have lower power consumption than their analog counterpart (If the loop bandwidth is small).

In summary, this research will cover three topics: A minimalist OOK transmitter with an on-chip resonator, the analysis of the optimal frequency of operation of systems with a constrained form factor, and an all-digital phase-locked loop.

1.2 Design Objectives

The target application of this work is WSN's with a fixed sensor position. In many situations, the sensor is already "embedded" in the environment. New buildings will have built-in sensors for temperature, humidity, vibrations etc., and their position is already defined. Given the small dimensions of the antenna and the possibility of implementing an on-chip array, a highly directive antenna solution at the receiver and the transmitter renders a better link budget used for enhancing the distance between the receiver and the transmitter and/or helps reducing the power consumptions when a minimalist Rx/Tx design is employed. An asymmetric master-slave network, Figure 1-1, will fit in our minimalist philosophy as the master device is mains operated and with high sensitivity and can transmit higher powers.

The slave TRx will point toward the master (can be the WLAN hub fixed in the ceiling) and the master device interrogates, in turn, each node in the WSN. Therefore, the slave

devices will not initiate data transfer. For WSN's with a smaller radius, one omnidirectional antenna integrated on-chip, will suffice.

As the slave devices will talk with the master, in turn, the chance of collision is zero. In this case, a preamble with the slave identification code will differentiate between the master device and slaves. In the master-slave topology in Figure 1-2, the strong attenuation and the poor sensitivity of the slave devices ensures non- collision between the slave nodes (The detection in the RX nodes will not respond to those weak signals).

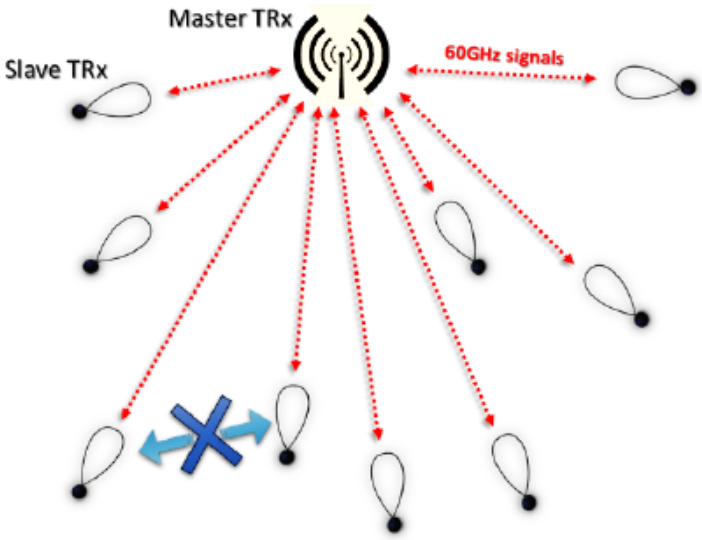


Figure 1-1 WSN with master/slave topology

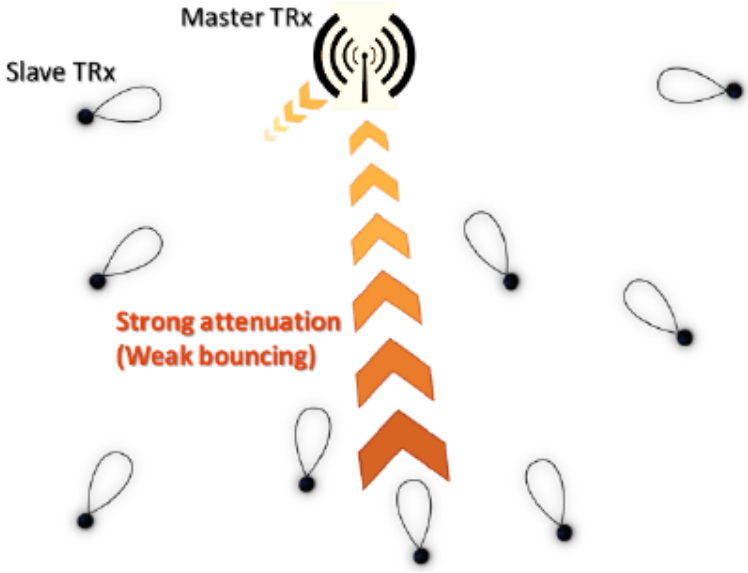


Figure 1-2 Weak bouncing due to high attenuation

1.3 Thesis organization

As stated earlier, this thesis discusses three main topics: A low power mm-wave transmitter with an on-chip resonator, a system level analysis of the optimal operating frequency for wireless sensor nodes with constrained form factor, and the design of an all-digital phase-locked loop (PLL). Chapter 2 begins with a literature review of transmitters and oscillators. In Chapter 3, the system level analysis is presented for the transmitter and receiver. Chapter 4 covers the design of passives used in the transmitter circuit. Chapter 5 describes the transistor level realization of the transmitter, the underlying principle of operation, and simulation results. Chapter 6 describes the design of the all-digital phase-locked loop. Chapter 7 concludes this work and future recommendations are presented. Finally, the appendix briefly describes a single stage LNA, which was designed, but then eliminated from the receiver circuit.

CHAPTER 2

State of the art: Transmitters and benchmark

2.1 Introduction

In this chapter, different transmitters from the literature are reviewed. The transmitters presented in Chapter 5 are based on a switched oscillator concept. Therefore, the benchmark is enhanced with most relevant oscillator designs.

2.2 A survey of transmitters in the literature.

As bits are sent in a WSN in an energy-constrained settings, the most important figure of merit is arguably the energy/bit or energy efficiency.

Figure 2-1 show the energy efficiency in J/bit for different designs, [2]-[16], for various data rates. The trend line from Figure 2-1 shows that going to higher data rates improves the energy efficiency. This is true as long as we neglect the turn on/turn off power and only the energy consumed for data transmission is considered.

The trend line in Figure 2-2 suggests that a better energy efficiency can be realized when increasing the carrier frequency. The lack of interferers, the existence of free bandwidth, and small antenna sizes are other incentives to attempt high energy efficiency transmitters at mm-wave frequencies.

Two transmitters designs are discussed in this thesis and both are highlighted (represented by the red square) in the Figure 2-1 and Figure 2-2 for different data

rates: 500Mbit/s, 10Mbit/s, and 100Kbit/s. However, Figure 2-1 and Figure 2-2 does not capture the most salient feature of our design. When sending a zero symbol, the oscillator based transmitter is switched off. On average, if zero and one symbols are equiprobable, the power consumption is halved. Figure 2-1 and Figure 2-2 report energy efficiency only when the transmitters are on.

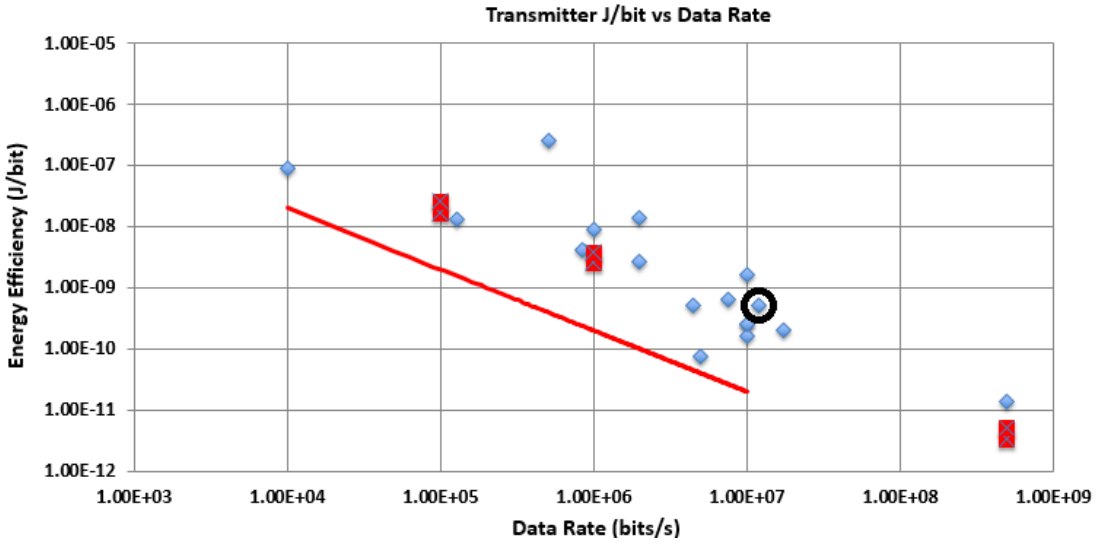


Figure 2-1 Transmitters energy efficiency vs. Data Rate

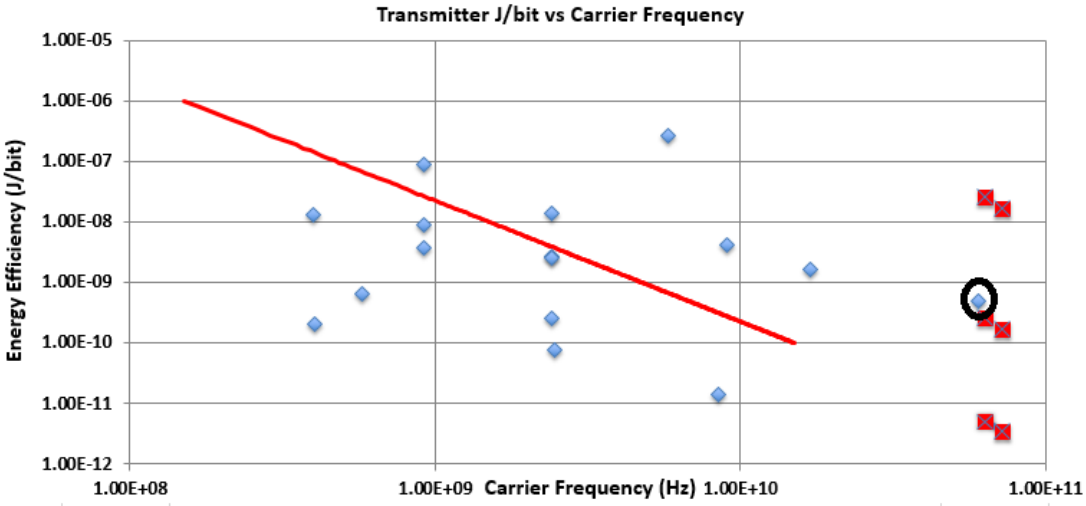


Figure 2-2 Transmitters energy efficiency vs. Carrier Frequency

As seen from Figure 2-2, most transceivers for wireless sensor network applications are located at low frequencies. At the time of writing this thesis, only one very recent paper, [16], discusses a 60GHz transceiver for wireless sensor

application. This paper demonstrates a fully integrated transceiver implemented using the 65nm CMOS technology and achieving an aggregated data rate of 12MBs. Although the transmitter presented in this paper, utilizes both a VCO and a PA, it can only deliver -3dBm of output power. Although not given in the paper, the power consumption estimated for the transmitter is 6mW. This design is circled in the last two figures.

2.3 Oscillators benchmark and literature review

In this section, a literature review of mm-wave oscillators is presented. Table 2-1 shows different designs found the literature with operating frequency, power consumption and output power.

A 60GHz Voltage Controlled Oscillator (VCO) using an on-chip resonator with an embedded artificial dielectric and implemented in 90nm CMOS was reported in [17]. In this design, artificial dielectric was employed to reduce the size, losses, and noise. A quality factor of 80 for the on-chip resonator, a power consumption of 1.9mW, and a phase noise of -100dBc/Hz at 1MHz offset were reported. The power consumption of the output buffer was not reported. The interesting feature of this design is the implementation of the high Q resonator. This resonator will be used in the transmitters implemented in this thesis as will be explained later.

In [18], a low phase noise CMOS VCO operating at 28GHz was reported, and the concept of amplitude redistribution was proposed. In this design, the power consumption is 14.4mW and the phase noise is -112.9 dBc/Hz at 1MHz offset. This design utilizes two filters, implemented using capacitors and inductors, needed for realizing amplitude redistribution. Amplitude redistribution attempts to keep transistors in saturation region which prevents the degradation in quality factor due to small load

MOSFET impedance when in the triode region. This technique is very useful to reduce phase noise, and another realization of amplitude redistribution will be investigated in this thesis.

An implementation of the amplitude redistribution technique described in [18], is given in [19]. The approach proposed in this paper is based on transconductance linearization to increase signal swing while reducing noise contribution from active devices. One of the two transmitter designs described in Chapter 5 is based on this design. This 24.7GHz oscillator achieves a phase noise of -127.3dBc/Hz @ 10MHz offset while consuming 36mW.

The 60GHz oscillator proposed in [20] achieves a phase noise of -87dBc/Hz at 1MHz with output power of -17dBm while consuming 24.6mA at a supply voltage of -3V.This deisgn is implemented in SiGe:C BICMOS technology. This means a power consumption of 73.8mW while driving a resistive load of 5.5Ω. The oscillator core in this design is a differential version of Colpitts oscillator. Although the output power is low, the power consumption is high and is not suitable for WSN applications.

A complete 60GHz transmitter, implemented in 0.18μm SiGe BiCMOS technology, is proposed in [21], where there is a 30GHz oscillator with a phase noise of -80.2dBc/Hz at 1MHz offset and consuming a power of at least 3.24mW. This design produces an output power of -8.5dBm. Even though the power consumption of this design is low, it does not include the power consumption of the frequency doubler. Similar implementation does not seem to be feasible for WSN due to the added power consumption of the frequency doubler.

A 60GHz Miller effect based VCO is proposed in [22] where the phase noise is -85dBc/Hz at 1MHZ offset. The output power reported is -13dBm. This design does not indicate power consumption, but according to the published figure of merit, the

power consumption can be estimated and is around 3mW. The concept presented here, employing Miller capacitance instead of conventional capacitors, aims to increase the tuning range rather than optimizing the output power of the oscillator. Hence, a similar implementation would not be useful for WSN targeted in this thesis.

In [23], a 59GHz Push-Push VCO for full band 60GHz transceiver is proposed. This design achieves a phase noise of -108dBc/Hz at 1MHz offset and produces an output of 1.2dBm while consuming 132mW. While the output power and the phase noise are good in this design compared to other designs, the power consumption is very high and is not suitable for ultra-low power applications. In this design, differential Colpitts oscillator is employed.

A 77GHz CMOS VCO with 6dBm output power and a phase noise of 88dBc/Hz at 1MHz offset is reported in [24]. In this design, the power consumption is around 190mW. This design utilizes a frequency doubler to obtain the 77GHz from a 38GHz oscillator. Moreover, this design achieves high output power by using a buffer and a preamplifier rendering the power consumption high. Due to its high power consumption, this design is not suitable for WSN applications.

A recent 60GHz frequency synthesizer that is based on extracting the second harmonic while preserving VCO performance is reported in [25]. The design achieves a phase noise of -118dBc/Hz at 10MHz offset and produces a maximum output power of 0dBm while consuming 66mW power.

In [26], a 60GHz frequency synthesizer is presented. The VCO part achieves a phase noise of -94.2dBc at 1MHz offset and -115dBc at 10MHz offset, and a power consumption of 11.4mW. The output power is not reported for this design. Since the output power is not indicated, it is not possible to determine if this design is adequate for WSN applications.

An AC-Coupled LC tank based 40GHz VCO is proposed in [27]. This design achieves a phase noise of -96dBc/Hz at 1MHz offset while consuming 70mW of power (24mW in VCO core). This design can operate at an ultra-low VDD of 0.5V consuming 8.4mW and producing an output power of -10dBm. The phase noise is not reported in this case. The concept presented in this work is useful to reduce VCO pushing and improving tuning range. Since the receiver is assumed to be broadband, both VCO pushing and tuning range are not of interest. While this design consumes relatively little power, the output power is low.

A dual-mode wideband reconfigurable oscillator is proposed in [28]. The frequency range of operation is 57-75 GHz. The power consumption is 13mW and the phase noise reported is -108dBc at 10MHz offset. The output power is not reported. Similar to [26], Since the output power is not reported, it is not possible to determine if this design is adequate for WSN applications.

In the transmitter proposed in [29], the VCO achieves a phase noise of -104dBc/Hz at 10MHz offset, producing an output power of -4dBm, while consuming 180mW of power, including the output buffer. This design attempts to achieve broad range rather than achieving low power consumption. Hence, it is suitable for applications with high data rates requirements.

From the previous literature review, it can be concluded that most oscillators are optimized for low phase noise or wide tuning range. Nevertheless, [17] introduces an interesting high - Q on-chip resonator and [18] presents a technique that promise low phase noise without a significant increase in power consumption. Both of which will be explored in an attempt to build low-power mm-wave transmitter.

A summary of the reviewed designs is shown in Table 2-1. One conclusion that can be drawn from this table is that oscillators in the literature are not optimized for

high output power. Both designs presented in this thesis are included at the end of the table.

Table 2-1 Literature review summary

Design	Operating frequency	Power consumption	Phase noise	Output power	Comment
[17]	60GHz	1.9mW	100 dBc/Hz @1MHz	-	Power consumption doesn't include output buffer power consumption
[18]	28GHz	14.4mW	-112.9 dBc/Hz @1MHz	-	Power consumption doesn't include output buffer power consumption
[19]	24.7GHz	36mW	127.3dBc/Hz @ 10MHz offset	-4.4dBm single ended output power	The numbers provided are PLL results in this paper
[20]	60GHz	73.8mW	-87dBc/Hz@ 1MHz	-17dBm	-
[21]	30GHz	3.24mW	-80.2dBc/Hz @1MHz	-8.5dBm	-
[22]	60GHz	3mW	-85 dBc/Hz @1MHz	-13dBm	Power consumption is estimated based on the figure of merit reported

[23]	60GHz	132mW	-108dBc/Hz @1MHz	1.2dBm	
[24]	77GHz	190mW	-88dBc/Hz@ 1MHz	6dBm	
[25]	56GHz	66mW	-118dBc/Hz @10MHz	0dBm	
[26]	60GHz	11.3mW	-94.2dBc @1MHz -115dBc@ 10MHz	-	
[27]	40GHz	70mW (26mW for VCO core) or 8.5mW in ultra-low power operation	-96dBc/Hz @1MHz when consuming 70mW	-10dBm when consuming 8.5mW	
[28]	57-75 GHz	13mW	-108dBc @10MHz offset	-	
[29]	74-89 GHz	180mW	-104dBc/Hz @10MHz	-4dBm	
Design 1	72.56GHz	3.3mW	90dBc/Hz @ 1MHz offset -117dBc/Hz	-2dbm	

			@ 10MHz offset.		
Design 2	64GHz	5mW	90dBc/Hz @ 1MHz offset -117dBc/Hz @ 10MHz offset.	2dbm	

CHAPTER 3

System level analysis

3.1 Introduction

In this chapter, the impact of form factor on the performance of the system in terms of energy efficiency of the entire system is investigated. Form factor restriction limits the size of the antenna, and we argue that this results in an optimal frequency of operation. The following analysis combines data reported in the literature, 3D electromagnetic simulations, and Friss transmission formula. Furthermore, the study was supported by designing 2 PCB antennas where s-parameter measurements were performed and checked to be consistent with the analysis.

Figure 3-1 shows data reported in the literature on different carrier frequencies and the corresponding energy efficiencies. At lower frequencies, such as the 2.4GHz ISM band, the antenna length is a few centimeters long. Using shorter lengths will result in a mismatch between the transmitter/receiver circuitry and the antenna, leading to inefficient transmission. This is caused by the degradation in radiation resistance if shorter lengths were used. While this might be solved by introducing matching circuits between the transmitter/receiver and the antenna, at higher frequencies, such as mm-wave frequencies, antenna mismatch becomes very critical and increasing the frequency becomes a necessity. At mm-wave frequencies, antenna dimensions become small, and it becomes possible to implement them on-chip. While higher frequencies can achieve better matching

when antenna dimensions are small, the power consumption of the receiver and the transmitter become higher at these frequencies. This could arguably be due to the higher current density required to speed the transistor or due to the difference in sensitivity.

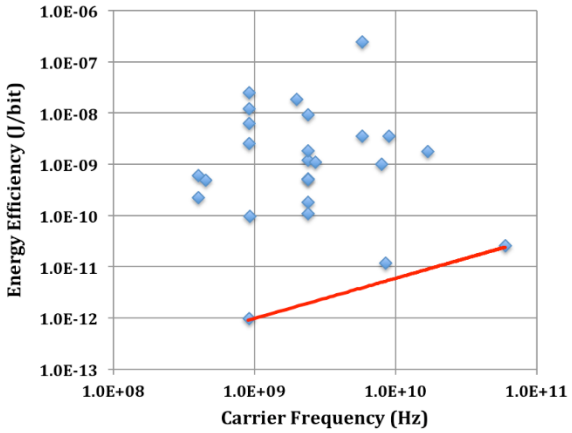


Figure 3-1 Receiver energy efficiency vs. carrier frequency

3.2 System model

The system model, which is shown in Figure 3-2, is composed of a power amplifier driving the antenna impedance, propagation between the transmitter and receiver that is governed by Friss transmission formula, and receiver antenna connected to a 50Ω load. In this analysis, the transmitter model is chosen to be analytical, unlike the receiver model that is chosen to be data driven.

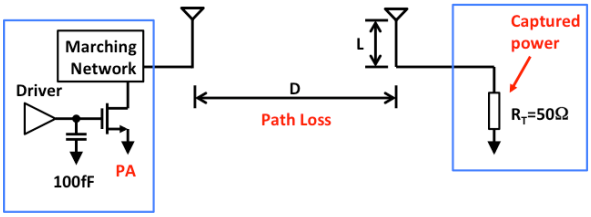


Figure 3-2 System model

On the transmitter side, half of the drain current is assumed to be used in driving the antenna. The power amplifier is considered to be a simple class-A amplifier. It is also assumed that the transmitter is on for only a very short period compared to

the receiver, which means that its impact on overall power consumption is limited most of the time.

The radiated power is given by:

$$P_{rad} = \left(\frac{P_{PA}}{V_{DD}}\right)^2 \frac{R_{ANT}}{4} \tag{3.1}$$

Where P_{PA} is the power consumption of the PA, V_{DD} is the supply voltage, and R_{ANT} is the half-wave dipole antenna radiation resistance [30].

$$R_{rad} = 20\left(\frac{\pi l}{\lambda}\right)^2 \tag{3.2}$$

Where l is the antenna length and λ is the wavelength. Using Friss transmission formula, it is possible to determine the power at the receiver side as follows [1]:

$$P_{RX} = P_{rad}\left(\frac{A}{D\lambda}\right)^2 \tag{3.3}$$

Where A is the antenna aperture that is assumed to be identical for the receiver and the transmitter sides, and D is the distance between the transmitter and the receiver. Now the captured power in the 50Ω receiver load is:

$$P_{RX} = 4P_{RX}\frac{50R_{ANT}}{50 + R_{ANT}} \tag{3.4}$$

Figure 3-3 shows a plot of published receivers vs. sensitivity which indicate that energy efficiency degrades by 10x for every 20dB improvement in sensitivity. Thus, from these published receivers and the trend shown in Figure 3-3 it is possible to derive the following for the receiver power consumption:

$$PWR_{RX} = 10^{-14}\frac{\text{Bit Rate}}{\sqrt{P_{CAP}}} \tag{3.5}$$

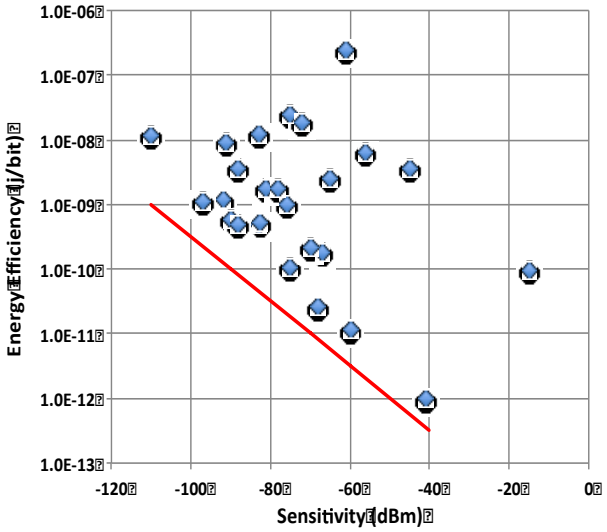


Figure 3-3 receiver energy efficiency vs. sensitivity

Based on the analytical model and the data published in the literature, it is possible to estimate the power consumption of the entire system as a function of the RF frequency. Figure 3-4 shows simulations result for three different antenna sizes: 1, 3, and 10mm, at a distance of 1 m between the transmitter and the receiver, and a power amplifier power consumption of 2mW. The supply voltage of the PA is assumed to be 0.3V so that the efficiency of the class-A power amplifier is improved. This supply voltage is feasible since the distance is small, and the transmitted signals are small. The input capacitance of the power amplifier is assumed to be 100fF, which must be driven by the previous stage. Moreover, it is assumed that for every 100 packets received, one packet is transmitted. Finally, the payload, which is assumed to be 1kb, is transmitted at a data rate of 1Mbps.

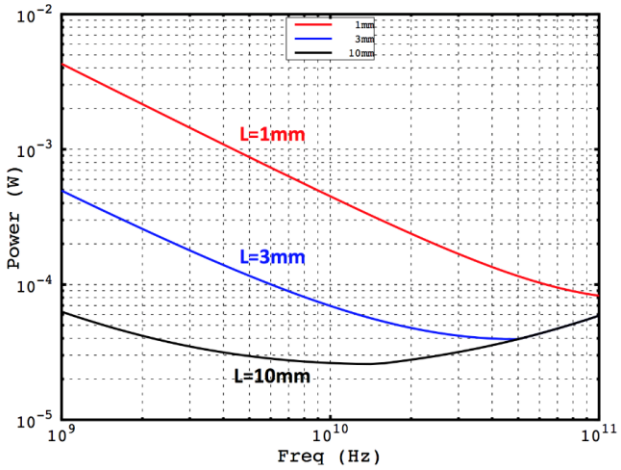


Figure 3-4 System power consumption vs. frequency

As the frequency increase, the antennas achieve better matching, and thus the power in Figure 3-4 improves. After reaching the point at which both antennas are matched, the length of the antenna can be decreased to maintain matching. Therefore, the receiver, and with it, the entire the entire system achieves lowest power when the captured signal at the receiver is highest. In Figure 3-4, it can be observed, the 10mm achieves lowest system power, due to its large size that result in lower receiver power consumption. In the case of the 10mm, the influence of the transmitter is more apparent, unlike the other two cases. The trend of Figure 3-4 suggests that higher frequencies allow for lower system power consumption when the antenna size is limited.

The effect of changing the data rate for a fixed 1kbit payload is shown in Figure 3-5 where the distance is assumed to be 1m, and the length of the antenna is 3mm. In the case of using a data rate of 1kbps, the receiver is enabled all the time and the power consumption is highest, while at higher data rates, the receiver is on for a shorter time, and the power consumption is lower. Moreover, for low data rates, the transmitter power consumption dominates system power consumption. The figure suggests that operating at higher data rates is beneficial in terms of total power consumption.

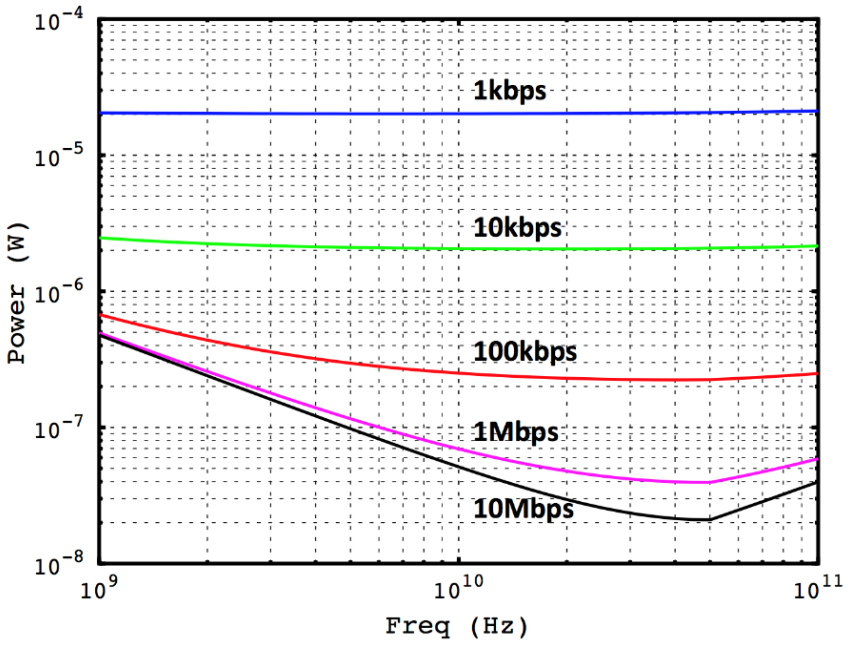


Figure 3-5 Impact of data rate on system power consumption

This model neglects many realistic limitations about of the on-chip antenna. To improve our model, a 3D electromagnetic simulator (HFSS) was used to characterize a 3mm antenna implemented on the top metal in a CMOS process technology. It is also assumed that the substrate thickness is 100μm with a resistivity of 10Ωcm.

S11 of the simulated on-chip antenna is shown in Figure 3-6 for which it is possible to see that matching point is around 32GHz. The gain vs. frequency of this antenna is shown in Figure 3-7. To account for the antenna gain on the system performance, the peak gain is used in Friss transmission formula.

The radiated, received, and captured powers for HFSS and analytical models are shown in Figure 3-8. Because antenna matching improves, the radiated power increase until 50GHz is reached, at which the radiation resistance is 50Ω, and the length of the antenna is decreased to keep impedance matching. The received power and the captured power improve until the frequency of the peak gain, around 32GHz, is reached and then starts degrading.

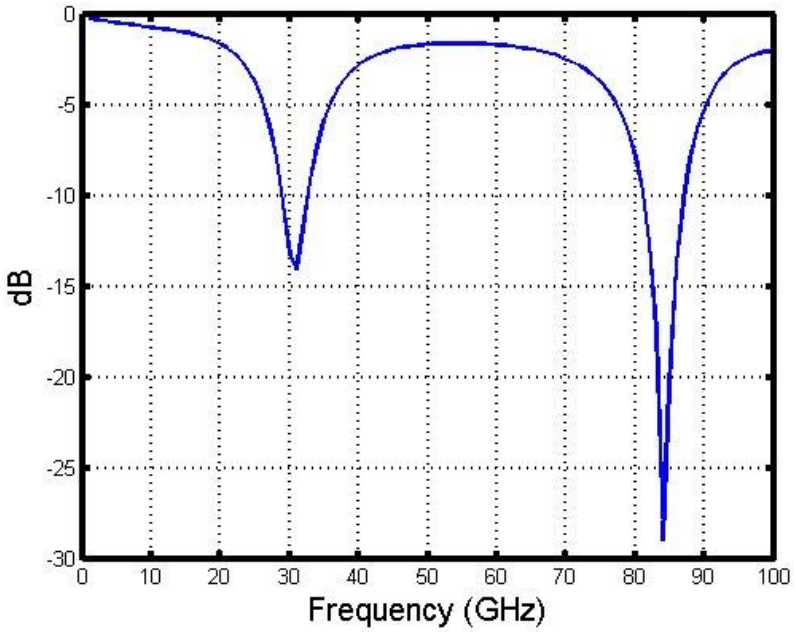


Figure 3-6 Simulated S11 of the on-chip antenna

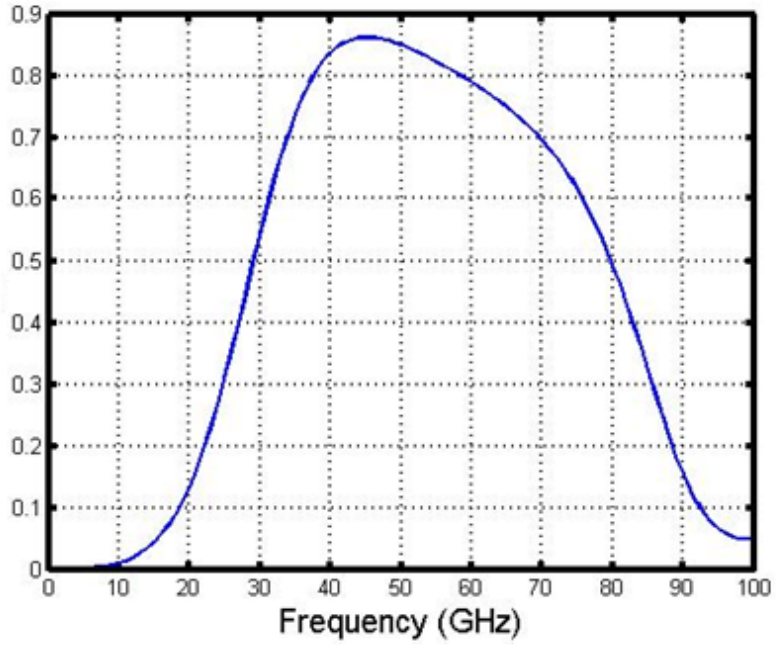


Figure 3-7 Simulated gain of the on-chip antenna

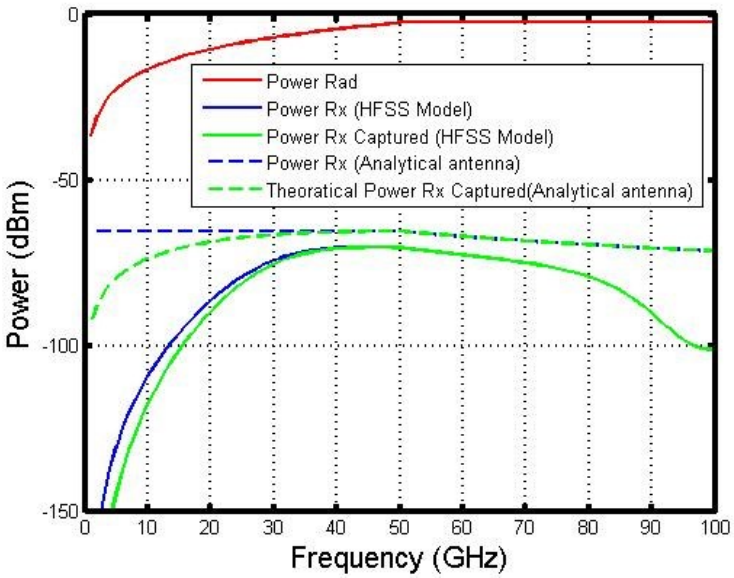


Figure 3-8 Radiated, received, and captured power

The power consumption of the HFSS and the analytical model are shown in Figure 3-9. Here, it is assumed that the data rate is 100kpbs.

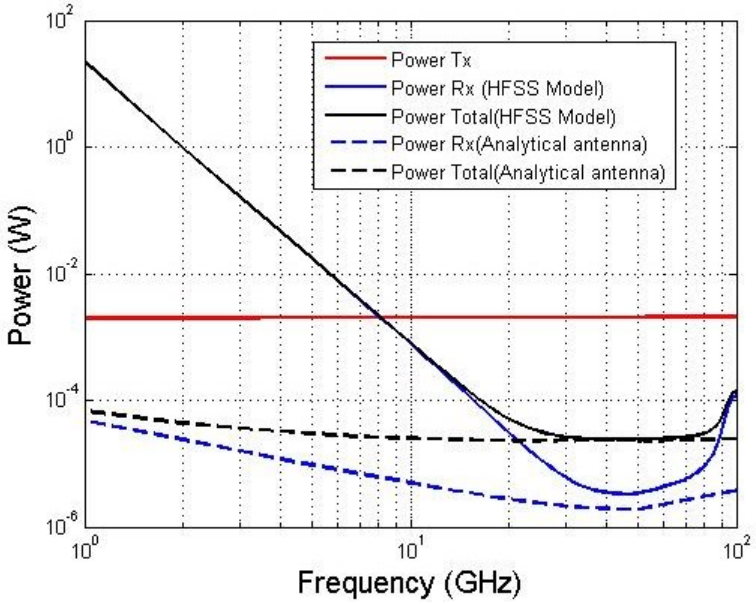


Figure 3-9 System power consumption

It is clear from the previous analysis that the best energy efficiency is when the captured power at the receiver is the largest which happens at the frequency which the antenna achieves matching. To validate this experimentally, the s-parameters, more specifically S_{21}, were measured using a network analyzer in the configuration

shown in Figure 3-10. Measurements using two simple monopole antennas centered at 5GHz and 15GHz were performed placed on a Rogers 4350B substrate to minimize losses.

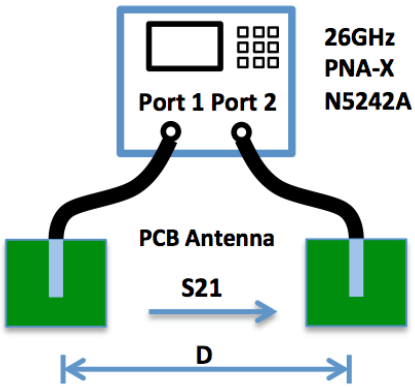


Figure 3-10 Experimental setup

S11, S22, S12 are all shown in Figure 3-11 and Figure 3-12 for the 15GHz and the 5GHz antennas respectively where the measurements were performed with a separation of 35cm between antennas. This mismatch between S11 and S22 is due to the connector positioning and soldering mismatch. In Figure 3-11, the peak around 12GHz is expected while the peak at 18GHz is likely due to the proximity of the connector. In Figure 3-12, there is only one peak at around 5GHz that is expected. The model correctly predicts the frequency at which the S21 peaks occur, i.e. maximum power transmission, which would be the optimal frequency of operation.

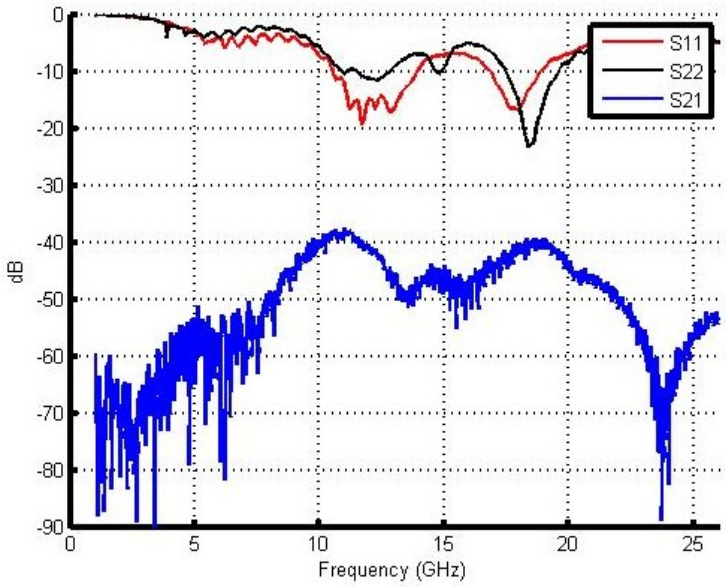


Figure 3-11 Measured s-parameters of 15GHz system

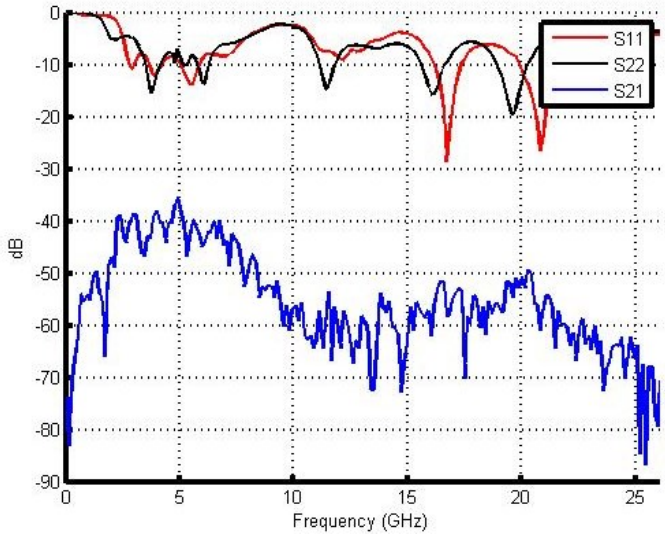


Figure 3-12Measured s-parameters of 5GHz system

In conclusion, the model developed succeeds in predicting the frequency of optimal energy efficiency operation. It also suggests that higher frequencies are favorable in systems with constrained form factor. Optimal energy efficiency is achieved at the frequency at which the largest antenna in the form factor achieves impedance match.

CHAPTER 4

60GHz on-Chip Resonator and Passives

4.1 Background

To obtain a low power, low phase noise oscillator, a resonator with a high quality factor is needed. HFSS was used to simulate the resonator and to obtain the quality factor. An on-chip resonator was simulated and implemented on-chip. The resonator implemented, shown in Figure 4-1, is a scaled version of the resonator proposed in [17]. The total length of the resonator is:

$$\lambda/4 + 25\mu m = 160\mu m$$

The width is 100 μm with each line having a width 25μm and with a spacing of 50 μm between both lines. The width of the piece of metal connecting both lines is 25μm as was used in the equation above. The spacing between conductive strips (not shown) beneath the resonator is 0.6μm.

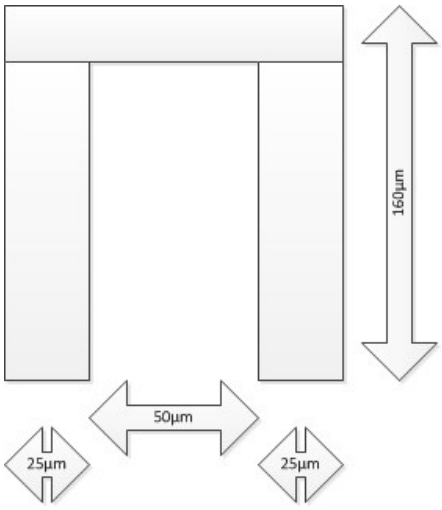


Figure 4-1 Resonator structure top view

Two-dimensional arrays of conducting strips (not shown in the figure) were placed underneath the resonator. These strips are embedded in a dielectric with permittivity constant ε. When an external electric field,E, is applied, the induced charge on strips results in polarization density P. In this case the displacement can be given by:

$$D = \epsilon E + P = \epsilon' E \tag{4.1}$$

Where $\boldsymbol{\epsilon'}$ is the effective permittivity of the artificial dielectric which is higher than permittivity constant ε.

This boost in the permittivity constant ε has several advantages. First, since the permittivity constant ε appears to be larger, it leads to a shorter resonator length, which in turn results in lower losses and higher Q factor of the resonator. This artificial dielectric reduced the length of the resonator from being 700µm to 150µm. Second, the current in the resonator flows in a direction perpendicular to the conducting strips, reducing the losses of the conductive strips. Third, the structure is shielded from the substrate through the conducting strips.

As will be explained in the oscillator design chapter, the resonator will be used in a differential configuration. Hence, since the resonator is a parallel resonator, high impedance should be seen when a differential signal is applied to the resonator. Figure 4-2 shows how the resonator admittance can be calculated when a differential signal is applied to the terminals of the resonator. Then the impedance can be given by[31]:

$$\mathrm{Z_{differential}} = \frac{2}{\mathrm{Y11} - \mathrm{Y12}} \tag{4.2}$$

Y-parameters can be extracted directly from EM simulations, and the rest of the calculation is straightforward. Figure 4-3 shows the differential impedance plotted against frequency.

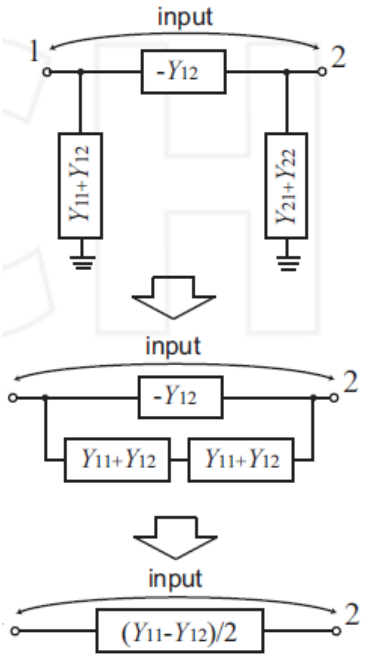


Figure 4-2 Resonator admittance (taken from [31])

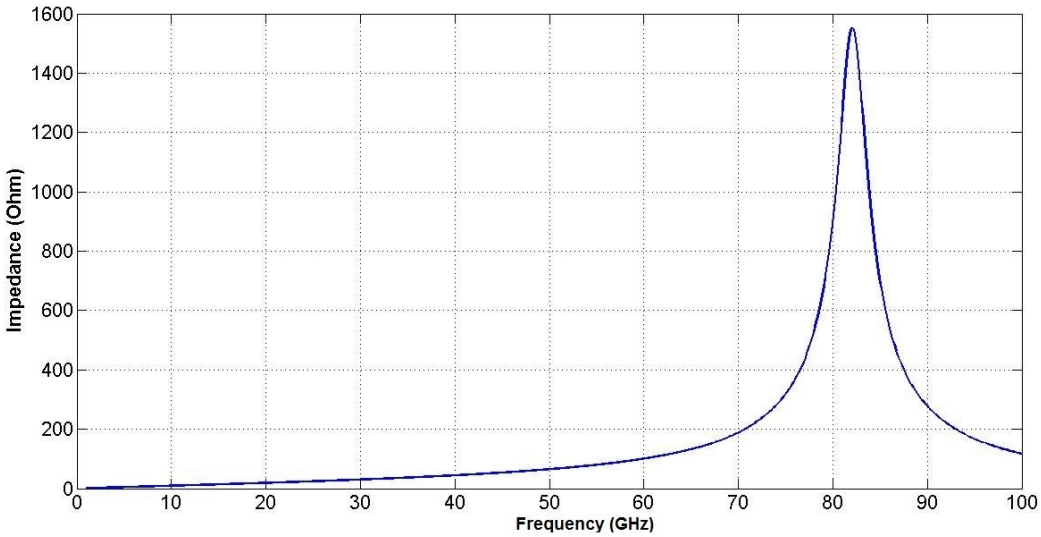


Figure 4-3 Resonator impedance against frequency

In Figure 4-3, the resonance frequency is higher than 60GHz. This was intentional because, as will be explained in the oscillator chapter, loading will cause the oscillation frequency to decrease to a lower frequency.

Many different methods are given for quality factor measurements in [32]. The 3dB method and the lumped model can be both used to obtain the quality factor of the resonator. Both methods are described below.

The 3dB method.

In this method, the plot S21 plotted vs. frequency is used to determine the quality factor. The frequency at which |S21| is maximum is the resonant frequency. The half power points ($\frac{1}{\sqrt{2}}\max S_{21}$) are determined on either side of the resonant frequency and the 3dB frequency difference ($\Delta f3dB$) which is the difference between these points can be determined. The quality factor is given by:

$$Q = \frac{f_o}{\Delta f3dB} \tag{4.3}$$

The lumped model method

In [32], the following equation is derived relating the quality factor and complex transmission coefficient:

$$Q = \frac{|\overline{S_{21}}|}{\sqrt{1 + 4Q^2(\frac{f}{f_o} - 1)^2}} \tag{4.4}$$

When S21 is known, it is possible to determine the quality factor by solving the last equation.

These are two generic methods for calculating the quality factor in all circuit configurations. Since the important parameter is the differential impedance, the 3dB

method will be applied, but using the curve shown in Figure 4-3 to estimate the quality factor. Carrying out the calculation, the quality factor obtained is around 17.

4.2 Capacitor design

HFSS EM simulator will be used to build capacitors to be used in the oscillators. The reason for using an EM simulator is to obtain better models at high frequencies. The methodology employed in the design of capacitors included the design of a unit capacitor of a small value of around 2.5fF and then through connecting multiple unit capacitors in series and parallel, it is possible to obtain all values needed. The unit capacitance has a high quality-factor of around 500.

Figure 4-4 shows 18 unit capacitors connected in parallel in order to obtain a value of around 45fF (18×2.5 fF $=$ 45fF). The plates of the capacitor are found in top metals. Moreover, in order to shield the capacitor from the substrate, a meshed ground plane was placed in bottom metal layer. This also helps in making the unit capacitance reproducible. The shape of the unit capacitance is chosen in a way that reduces lateral capacitance which gives a better prediction of the final value of the capacitor, and also to make the connection with other unit capacitances more convenient.

The left side of Figure 4-5 [31] shows how the Y-parameters can be used to describe the capacitor when connected in a single-ended configuration, while the right side of the same figure shows how the Y parameters can be used to describe the capacitor when connected in a differential configuration.

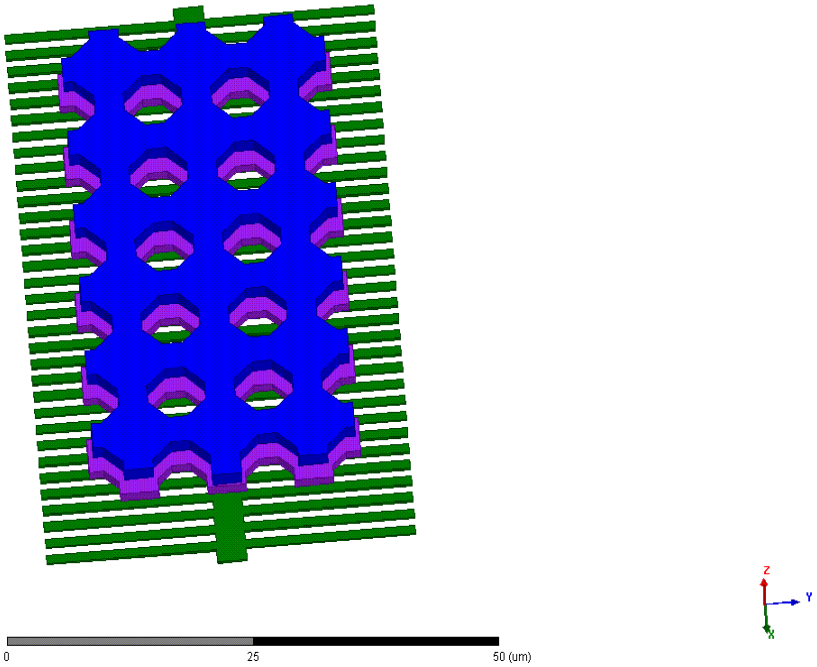


Figure 4-4 45fF capacitor

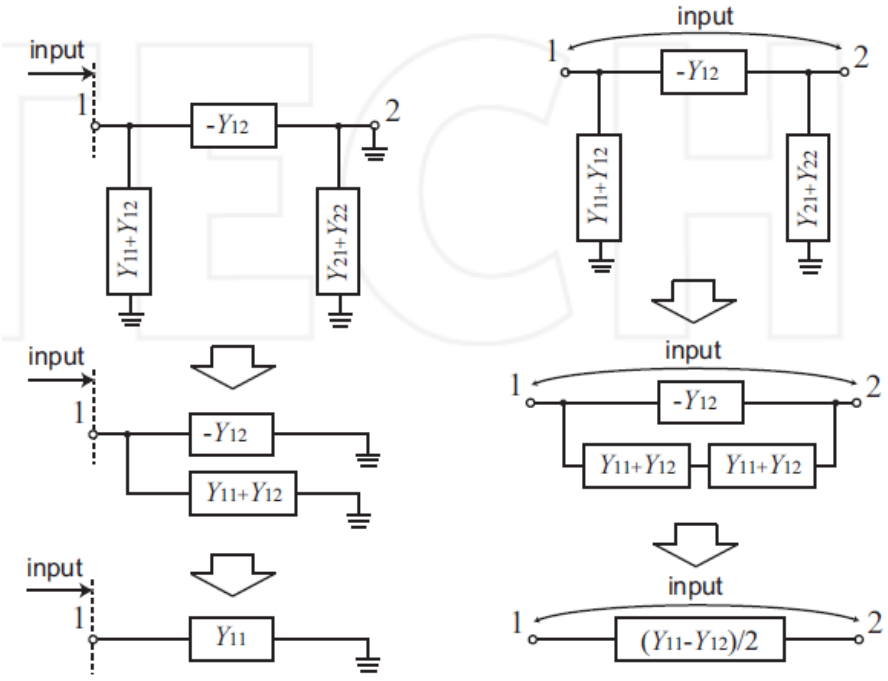


Figure 4-5 Capacitor characterization (Taken from [31])

A 2 port simulation of the capacitor can produce s-parameters that then can be converted to Y-parameters. The value of the capacitance can be directly derived from Y-parameters for the single-ended case through the use of the equation[31]:

$$C_{single\ endded} = \frac{Im(Y11)}{2\pi f} \tag{4.5}$$

while in the differential configuration case, the following equation was used[31]:

$$C_{differential} = \frac{\frac{Im(Y11 - Y12)}{2}}{2\pi f} \tag{4.6}$$

In both cases, the value of the capacitance obtained closely matched the estimated value, $18 \times 2.5\ \text{fF} = 45\text{fF}$, and each other's. Figure 4-6 shows the value obtained for the capacitor shown in Figure 4-5. All other capacitors were designed using this methodology.

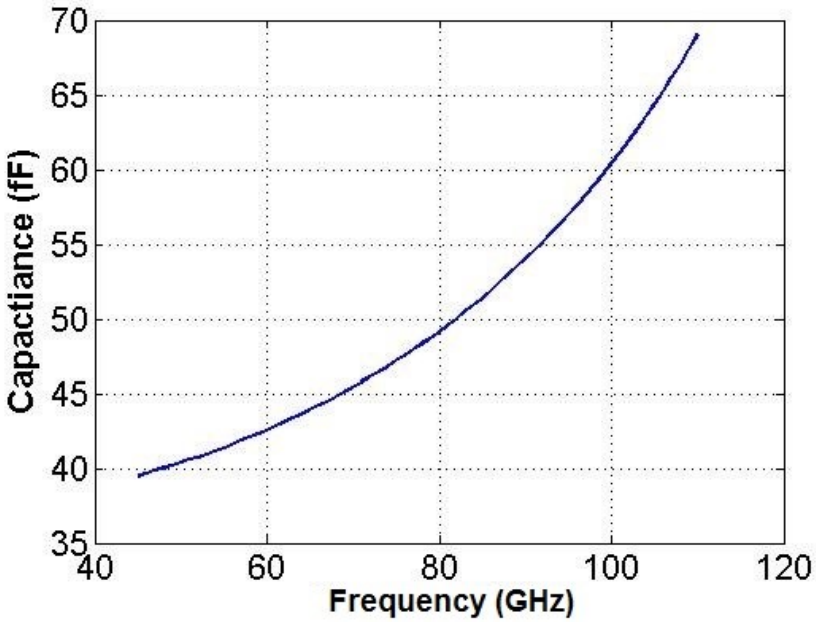


Figure 4-6 Capacitor simulation

It is worth mentioning that large values of capacitance have lower quality factor and could suffer from self-resonance frequency. Using the same methodology described above for the design of a 100fF capacitor, Figure 4-7 shows the value of

capacitance obtained plotted against frequency. It can be seen while the value of the capacitance obtained is correct at 60GHz, the self-resonance frequency is around 85GHz.

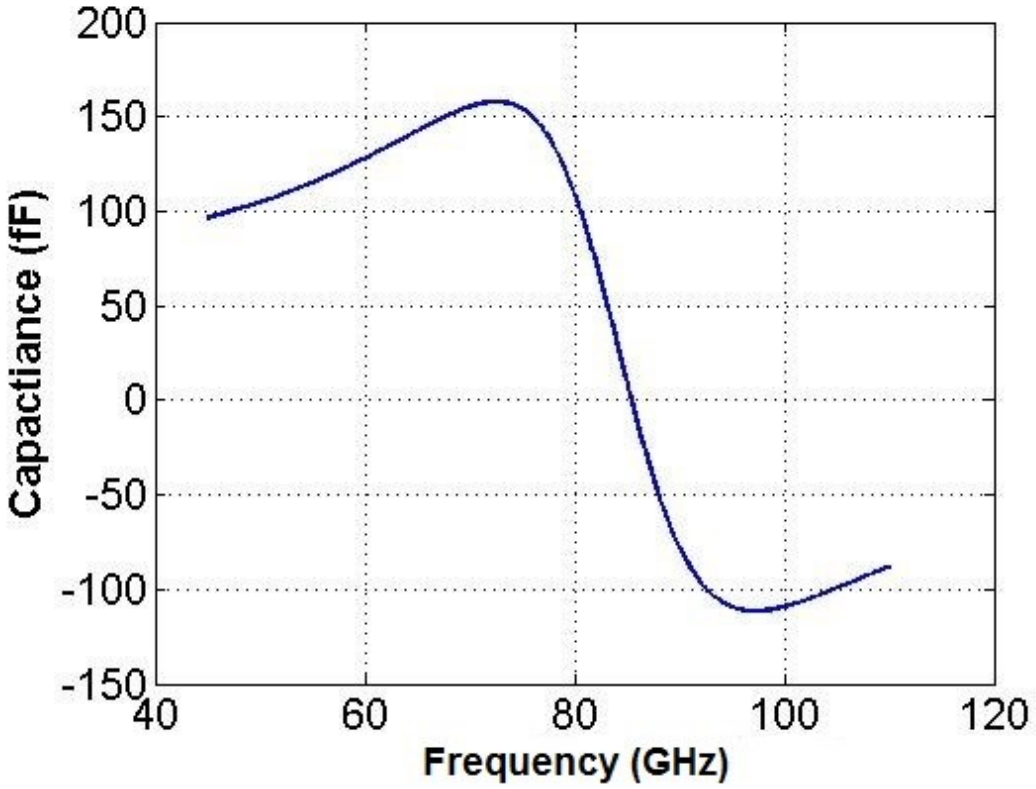


Figure 4-7 100fF Capacitor simulation

4.3 Inductor design

Similar to the case of the capacitor, inductors will be designed using EM simulators in order to obtain accurate models. Moreover, since the minimum available inductor found in the library is around 220pH, and the value needed is 80pH, EM simulators were used to design the inductors.

The inductor design is shown in Figure 4-8. The body of the inductor is located on the top metal layer, LB, while being shielded from the substrate through the use of a meshed ground plane found on the lowest metal layer, M1. The supply voltage will be connected through the center tap of the inductor. Thus, a three port model is needed

for the inductor. EM simulators were used to obtain Y-parameters where they were used in the model shown in Figure 4-9 [31].

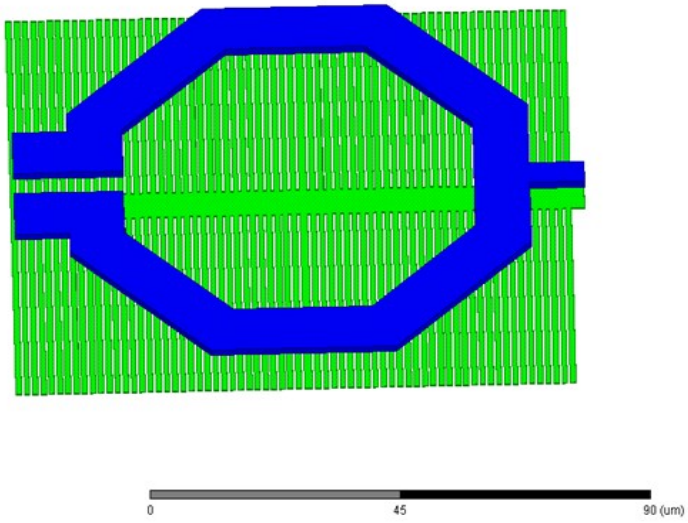
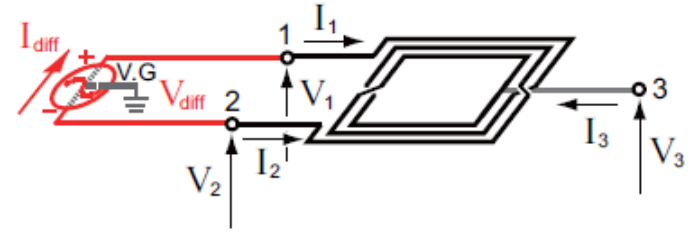


Figure 4-8 80pH inductor



$$I_1 = -I_2 = I_{diff}, \quad I_3 = I_x, \quad V_1 = -V_2 = V_{diff}/2, \quad V_3 = V_x$$

$$\begin{pmatrix} I_{diff} \\ -I_{diff} \\ I_x \end{pmatrix} = \begin{pmatrix} Y_{11} & Y_{12} & Y_{13} \\ Y_{21} & Y_{22} & Y_{23} \\ Y_{31} & Y_{32} & Y_{33} \end{pmatrix} \cdot \begin{pmatrix} V_{diff}/2 \\ -V_{diff}/2 \\ V_x \end{pmatrix}$$

$$V_{diff} = \frac{2\cdot(Y_{23}+Y_{13})I_{diff}}{Y_{23}(Y_{11}-Y_{12})-Y_{13}(Y_{21}-Y_{22})} = Z_{diff}\cdot I_{diff}$$

$$\therefore L_{diff} = \frac{1}{\omega}\mathrm{Im}(Z_{diff})$$

$$Q_{diff} = \frac{\mathrm{Im}(Z_{diff})}{\mathrm{Re}(Z_{diff})}$$

Figure 4-9 3-port model of the inductor (Taken from[31])

Simulation results for the inductor shown in Figure 4-8 are shown in Figure 4-10. It is evident from the figure the inductance value is around 80pH, and the peak quality factor of around 15 is centered around 55GHz.

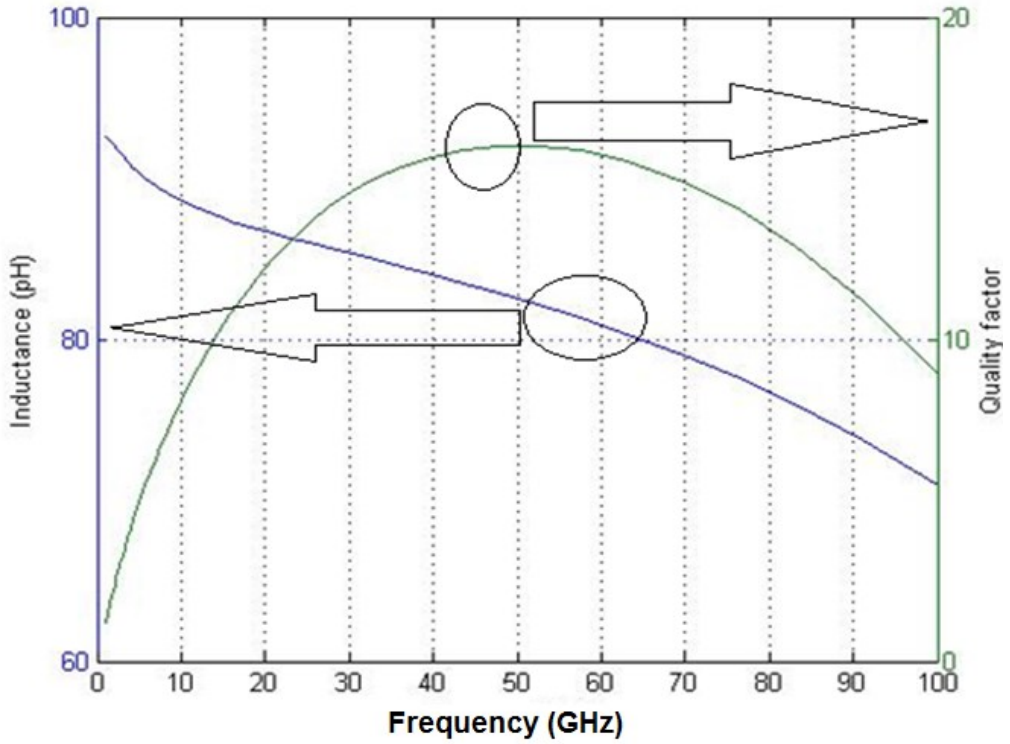


Figure 4-10 Inductor simulated

CHAPTER 5

Oscillator and Transmitter Design

5.1 Specifications

As wireless sensor nodes are limited in size, a small antenna is required. Hence, the operating frequency should be high in order for the antenna size to be as small as possible. Moreover, since the receiver is naturally broadband and is capable of operating in the range of 50 – 70 GHz, a reasonable target would be a transmitter capable of transmitting at an **operating frequency of 60GHz**. Furthermore, as the receiver can detect binary amplitude modulated data, an On-Off keying transmitter will be targeted. In terms of the load, the transmitter needs to drive, a 50Ω. Finally, the power consumption of the power amplifier is high, it will be eliminated in the transmitter architecture, and a switched load will directly drive **50Ω loads – in differential output configuration.** Thus, the target power consumption set is **a power consumption less than 10mW** while delivering output power of **-3dBm to a single-ended a 50Ω load.**

A summary of the specification is shown below for the transmitter:

- Operates at a frequency of 60GHz.
- Drives 50Ω loads – in differential output configuration.
- Delivers -3dBm to each single ended a 50Ω load.
- Consumes power less than 10mW for the entire transmitter.

5.2 Oscillator design

The amplitude redistribution technique proposed in [18] is used to improve the phase noise of cross-coupled oscillators through the control of voltage swings on the gate and the drain nodes of the oscillator transistors. This pushes going into the triode region to higher drain voltages. In other words, the large signal transconductance,Gm, vs. gate amplitude voltage becomes linear. The reason for phase improvement is that when the transistors are kept in the saturation region, the degradation in the quality factor is avoided. Stated in another way, when the transistor enters triode region, the quality factor is degraded due to low impedance of the transistor in the triode region, and this is avoided by keeping the transistor in the saturation region.

The technique proposed for implementing amplitude redistribution concept is through the use of drain and gate capacitive dividers. To illustrate the concept, we first consider the feedback model of the simple crossed coupled oscillator and its simple half circuit shown in Figure 5-1. From the figure it is seen that when the drain terminal of one transistor is connected to the gate of the other. This implies that higher drain voltages needed to deliver higher output power will result in higher gate voltages that will cause the transistor to enter triode region degrading phase noise.

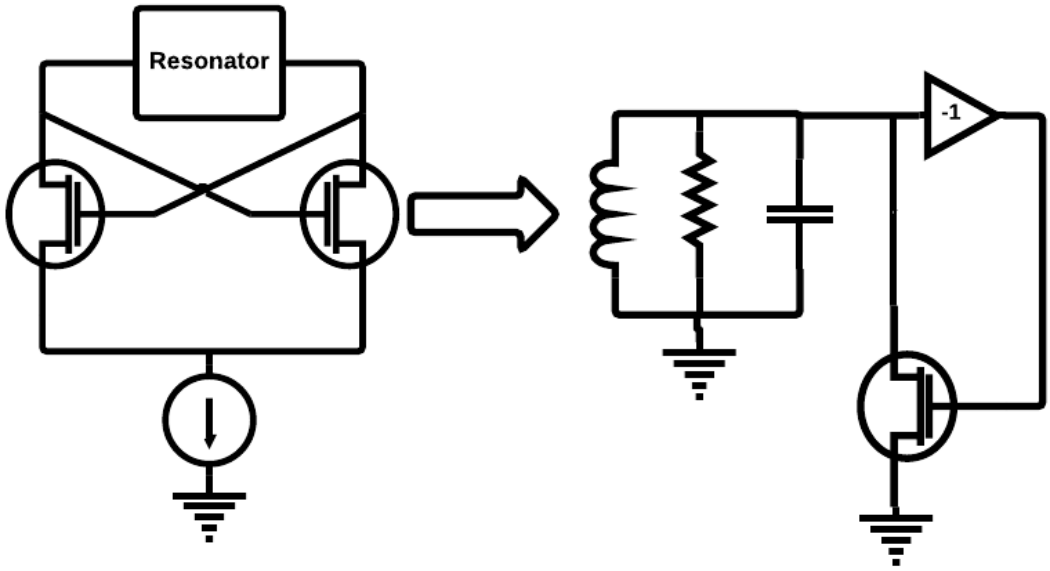


Figure 5-1 Cross-coupled oscillator

To implement amplitude redistribution, partial feedback is employed as shown in Figure 5-2. Employing this partial feedback enables the transistor to stay in saturation region at higher gate voltages.

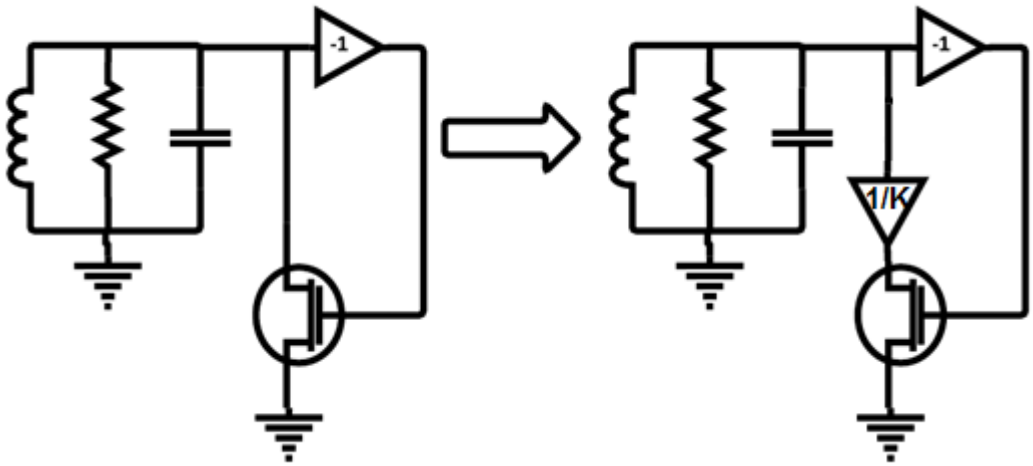


Figure 5-2 Partial feedback

Employing partial feedback technique improves the effective transconductance of the transistor. This is seen from the small signal analysis of the models shown in Figure 5-3.

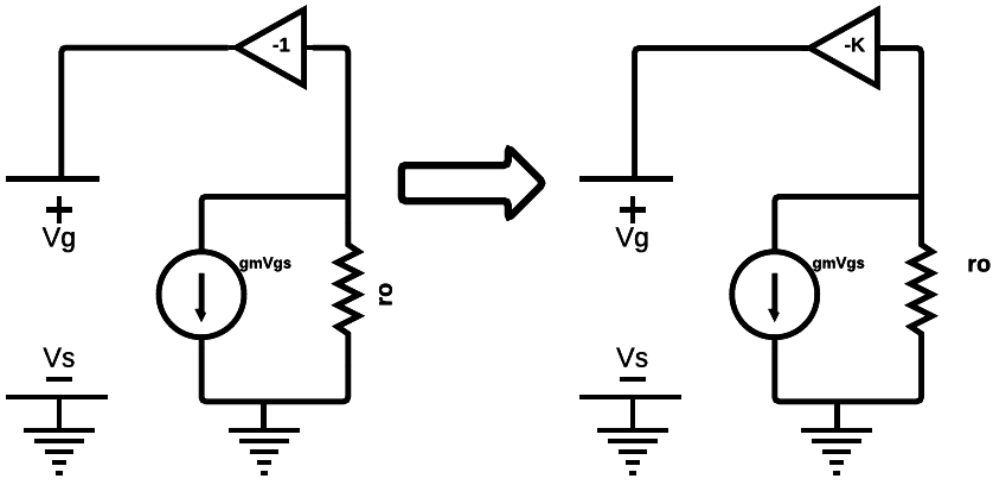


Figure 5-3 Small model for direct and partial feedback

The effective small signal conductance is improved in the case of partial feedback. The small signal transconductance for both instances are:

$$gm, eff = gm - \frac{1}{r_o} \tag{5.1}$$

$$gm, eff = gm - \frac{1}{K\, r_o} \tag{5.2}$$

From this, it can be concluded that the large signal transconductance is both boosted, due to the boost in the effective transconductance, and linearized resulting in a lower phase noise.

The schematic for the circuit employing this technique is shown in Figure 5-4, which is a design based on the oscillator described in [19]. Before embarking on the analysis of this circuit, a few observations can be made. First, the tail MOSFET transistor is switched on and off by data to turn on and off the oscillator and thus archiving OOK modulated signal. Second, it can be seen that the antenna is driven directly by the oscillator on one side, and a 50Ω dummy load is connected on the other side. Third, the bias voltage is applied through the center tap of the resonator. Finally,

the transmission line, which is used to realize an inductor, is connected in series with the tail MOSFET to cancel the effect of the capacitance added by the tail MOSFET.

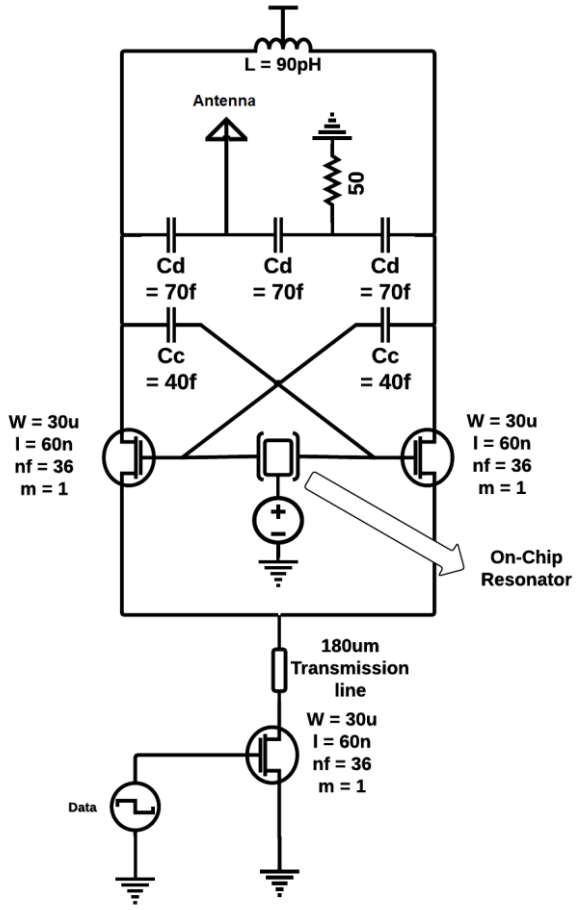


Figure 5-4 Partial feedback switched oscillator

The feedback model for this circuit is shown Figure 5-5. The next step is to derive the small signal effective transconductance that will be the upper limit of the large signal transconductance. The small signal model is shown in Figure 5-6. From the small signal model, the voltage division factor, 1/K, can be approximated:

$$\frac{1}{K} \approx \frac{Cc}{Cd + Cc} \tag{5.3}$$

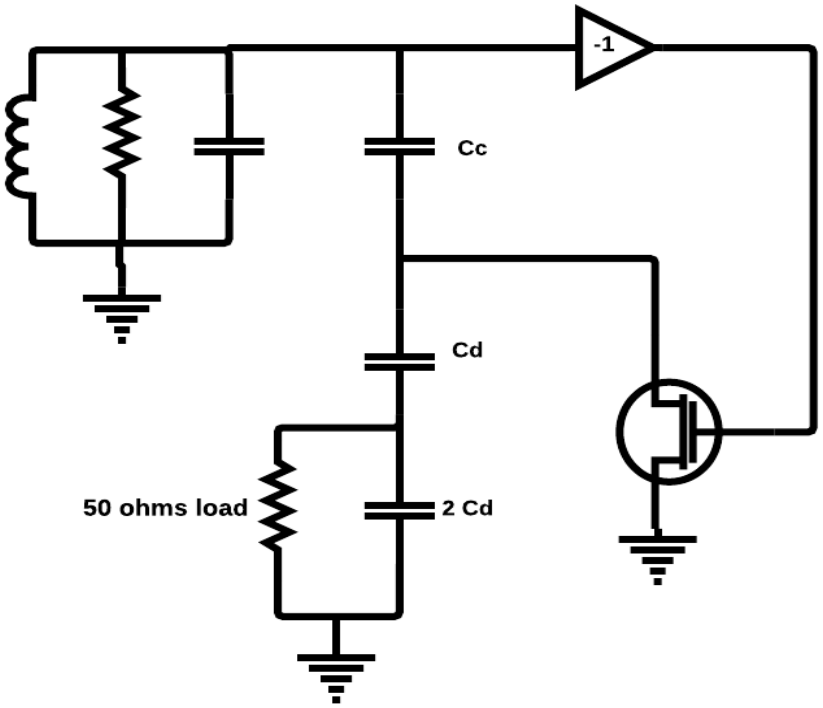


Figure 5-5 Feedback model for oscillator partial feedback oscillator

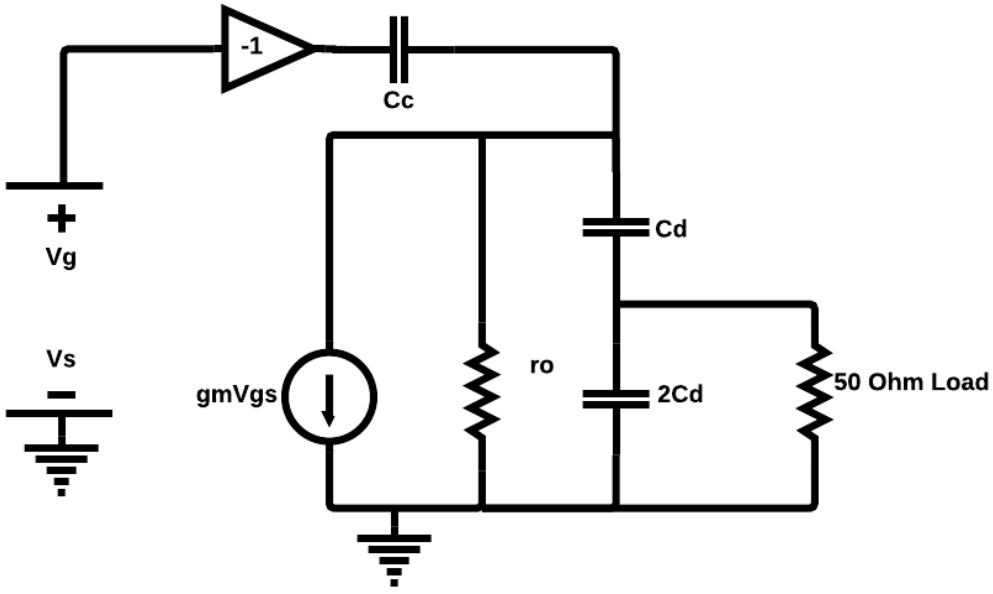


Figure 5-6 Partial feedback small signal model

Finally, the effective small signal transconductance is:

$$\mathrm{gm,eff} \approx \mathrm{gm} - \frac{\mathrm{Cc}}{(\mathrm{Cd} + \mathrm{Cc})\, \mathrm{r_o}} \tag{5.4}$$

One conclusion that can be drawn from the last equation is that the smaller the value of Cd, the higher the effective transconductance. This fact suggests that the smaller the value of Cd, the less apparent the effect of loading the oscillator with antenna and the dummy load, assuming that both the antenna and the dummy load are fixed. Simulations support this conclusion. It is true that a large value of Cc yields similar result, but the value of this capacitor essential to determining the frequency of oscillation.

As mentioned earlier, the effective transconductance is boosted. However, as can be seen in Figure 5-5, only part of the MOSFET current flows into the tank. Thus, the large signal transconductance seen by the tank,$G_{\mathrm{m,tank}}$, is reduced. The fraction of the drain current flowing in the tank is given by [19]:

$$It = \frac{Id}{n} \tag{5.5}$$

where

$$n = \frac{Z_{Cd} + Z_{Cc} + R_t}{Zcd} = \frac{Cc + Cd + Rt.s.Cd.Cc}{Cc} \tag{5.6}$$

The large signal transconductance vs. gate amplitude is plotted in Figure 5-7 (taken from [19]) for the case of cross-coupled oscillator and the linearized oscillator. In this figure, the curve marked I is for the case of cross-coupled oscillator, where II and III are for the case of linearized oscillator. Here, III is the large signal transconductance seen by the resonator. The steady swing occurs when the large signal transconductance is equal to the losses of the resonator, i.e. Gm x Rt = 1.

Some conclusions can be drawn from this Figure 5-7. First, the figure shows that the large signal transconductance is linearized compared to the simple cross-coupled case. Second, it is possible to see the increase in swing compared to the simple

cross-coupled oscillator. Third, the large signal transconductance seen by the tank is reduced which means improved phase noise performance,

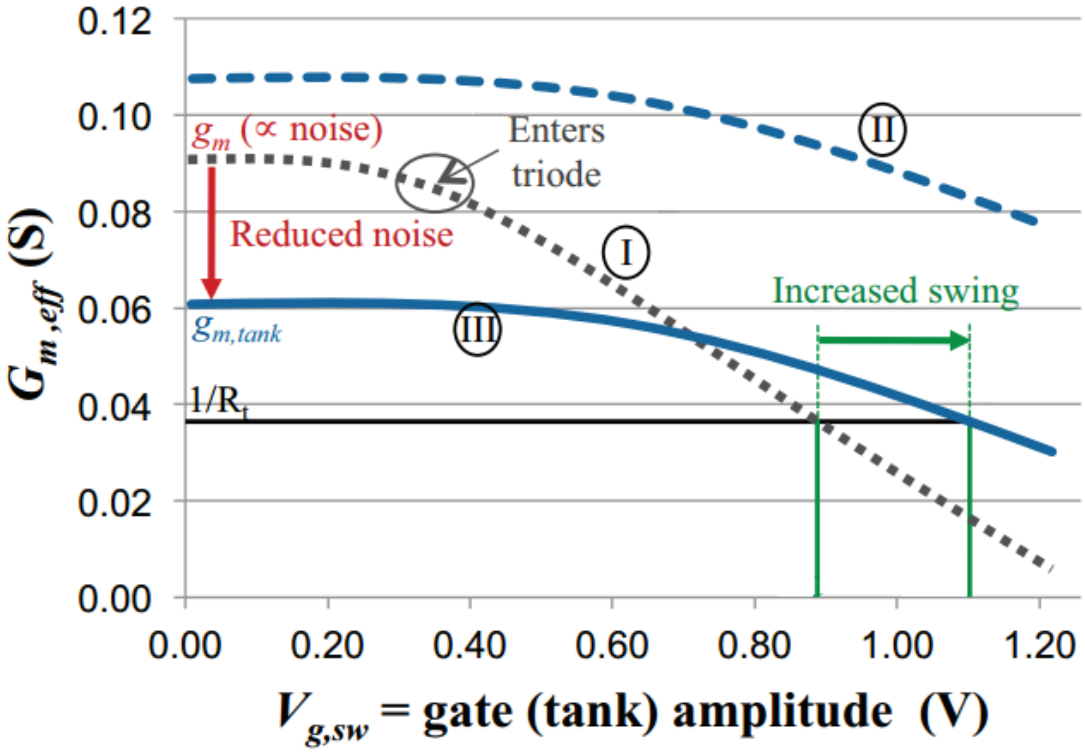


Figure 5-7 Transcoductance linearization (taken from [19])

To better understand the effect of loading and also to see the negative resistance that the active circuit provides, the model shown in Figure 5-8 is used to derive the value of the impedance.

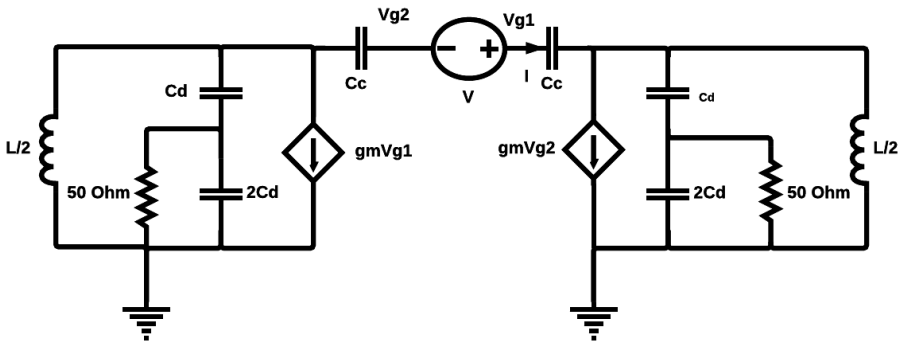


Figure 5-8 Model for calculating impedance seen by the resonator

With a little labor, the impedance seen by the resonator is given by:

$$Z = \frac{2(\frac{Z_s}{Z_L} + 1)}{\frac{1}{Z_L} - gm} \tag{5.7}$$

Where

$$Z_s = \frac{1}{sC_c} \tag{5.8}$$

And

$$Z_L = (R_{ant} \;//\; \frac{1}{2sCd} + \frac{1}{sCd}) \;//\; \frac{sL}{2} \tag{5.9}$$

It easily can be seen that for the case of simple cross-coupled oscillator, where $Z_s = 0$ and $Z_L = \infty$, the impedance equation simplifies to the known equation

$$Z = \frac{-2}{gm} \tag{5.10}$$

Going back to the impedance equation, we will simplify the expression in two components: the negative resistance and the value of the capacitance loading the resonator and thus reducing the oscillation frequency.

First, we look at the combination of Cd, 2Cd, and the resistance R. At sufficiently high frequencies, the admittance is given by:

$$G = \frac{1}{n^2 R} = \frac{1}{9 R} \tag{5.11}$$

where

$$n = \frac{Cd + 2Cd}{Cd} = 3 \tag{5.12}$$

and the susceptance, again at sufficient high frequencies, is:

$$Bin = \omega \frac{Cd \times 2Cd}{Cd + 2Cd} = \frac{2}{3}\omega Cd \tag{5.13}$$

Hence, the total admittance of that part is given by:

$$Y = \frac{1}{9 R} + j\frac{2}{3}\omega Cd \tag{5.14}$$

Now, it possible to add the inductor effect to the equation:

$$Y = \frac{1}{9\,R} + j\frac{2}{3}\omega Cd - \frac{2j}{\omega L} = \frac{1}{9\,R} + j2(\frac{1}{3}\omega Cd - \frac{1}{\omega L}) \tag{5.15}$$

The value of the real part of the previous equation is very small compared to the imaginary part for reasonable design values and will be neglected. Hence, the last equation becomes:

$$Y = j\frac{2}{3}\omega Cd - \frac{2j}{\omega L} = 2j(\frac{1}{3}\omega Cd - \frac{1}{\omega L}) \tag{5.16}$$

Finally, Z_L can be approximated as

$$Z_L \approx \frac{-j}{2\,(\frac{1}{3}\omega Cd - \frac{1}{\omega L})} \tag{5.17}$$

Now substituting the value back into the impedance seen by the resonator (eq 5.7) we get:

$$Z = \frac{2(2j(\frac{1}{3}\omega Cd - \frac{1}{\omega L}) \times \frac{1}{j\omega C_c} + 1)}{2j(\frac{1}{3}\omega Cd - \frac{1}{\omega L}) - gm} \tag{5.18}$$

which simplifies to

$$Z = 2(2(\frac{1}{3}\omega Cd - \frac{1}{\omega L}) \times \frac{1}{\omega C_c} + 1)\ \frac{-2j(\frac{1}{3}\omega Cd - \frac{1}{\omega L}) - gm}{(2\left(\frac{1}{3}\omega Cd - \frac{1}{\omega L}\right))^2 + gm^2} \tag{5.19}$$

Finally, it is very easy to see the imaginary and the real parts of the impedance seen by the resonator:

$$Real(Z) = 2(2(\frac{1}{3}\omega Cd - \frac{1}{\omega L}) \times \frac{1}{\omega C_c} + 1)\ \frac{-gm}{(2\left(\frac{1}{3}\omega Cd - \frac{1}{\omega L}\right))^2 + gm^2} \tag{5.20}$$

$$imaginary(Z) = 2(2(\frac{1}{3}\omega Cd - \frac{1}{\omega L}) \times \frac{1}{\omega C_c} + 1)\ \frac{-2j(\frac{1}{3}\omega Cd - \frac{1}{\omega L})}{(2\left(\frac{1}{3}\omega Cd - \frac{1}{\omega L}\right))^2 + gm^2} \tag{5.21}$$

The real part is a negative resistance provided by the active circuit, while the imaginary part is the capacitance added by the active circuit which will cause the frequency of oscillation to reduce.

In conclusion, this configuration fulfills the required conditions for oscillation and also provides a technique to improve the phase noise.

5.3 Startup condition and oscillation frequency

The Barkhausen stability criterion will now be used to determine the oscillation frequency and startup conditions. First, the small signal gain of a single stage will be derived. Then, this value will be used when the Barkhausen stability criterion is applied and the starting and the oscillation frequency can be determined.

The analysis is started by considering the circuit shown in Figure 5-9. The combination of Cd, 2Cd, the 50Ω load, and the inductor with inductance of L/2 were represented by Z_L in the previous derivation and will be used here. All assumptions remain correct here and thus the value of this combination is repeated here as:

$$Z_L \approx \frac{-j}{2\left(\frac{1}{3}\omega Cd - \frac{1}{\omega L}\right)} \tag{5.22}$$

Lr, Cr, and R loss are the resonator inductance, capacitance, and resistance. Now the small signal gain can be determined as:

$$\frac{Vo}{Vi} \approx gm \frac{\frac{-j}{2\left(\frac{1}{3}\omega Cd - \frac{1}{\omega L}\right)} \times \left(\frac{1}{j\omega Cc} + \frac{j\omega Lr}{(1-\omega^2 LrCr) + \frac{j\omega Lr}{Rloss}}\right)}{\frac{-j}{2\left(\frac{1}{3}\omega Cd - \frac{1}{\omega L}\right)} + \frac{1}{j\omega Cc} + \frac{j\omega Lr}{(1-\omega^2 LrCr) + \frac{j\omega Lr}{Rloss}}} \tag{5.23}$$

To satisfy the Barkhausen criterion, and since there are two identical stages, the phase of the last equation should be set to 180 degrees. Moreover, the gain should be larger than one for proper startup.

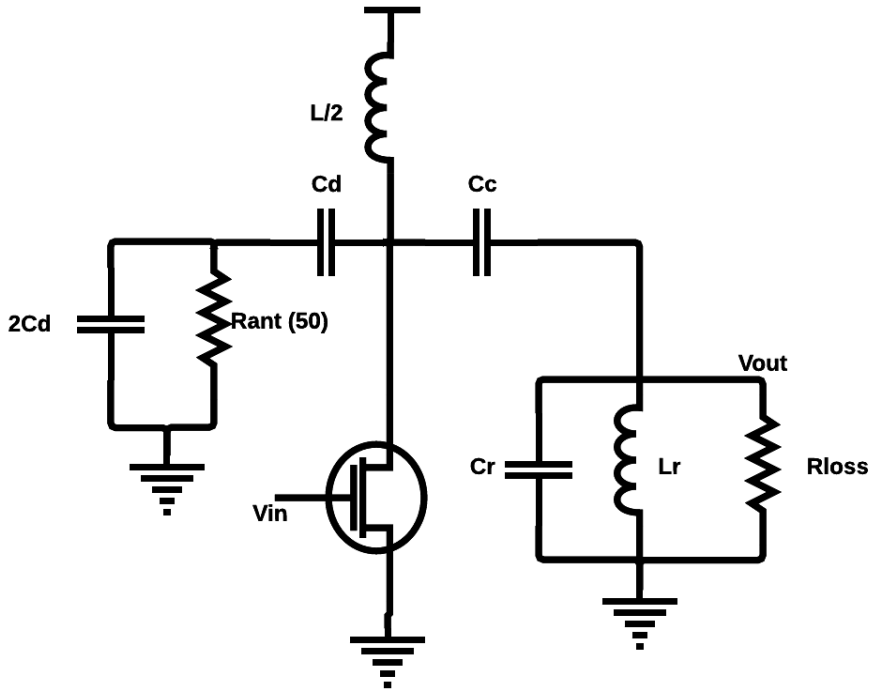


Figure 5-9 Circuit used for open loop gain derivation

5.4 Low voltage Colpitts oscillator

A second implementation of the transmitter is shown in Figure 5-10. Before embarking on the analysis of this circuit, a few observations can be made. First, the tail MOSFET transistor is switched on and off by the data to turn on and off the oscillator and thus archiving OOK modulated signal. Second, it can be seen that the antenna is driven directly by the oscillator on one side, and a 50Ω dummy load is connected on the other side. Third, the bias voltage is applied through large resistors to the gates of the four transistors as shown in Figure 5-10. Finally, and transmission line, which is used to realize an inductor, is connected in series with the tail MOSFET to cancel the effect of the capacitance added by the tail MOSFET.

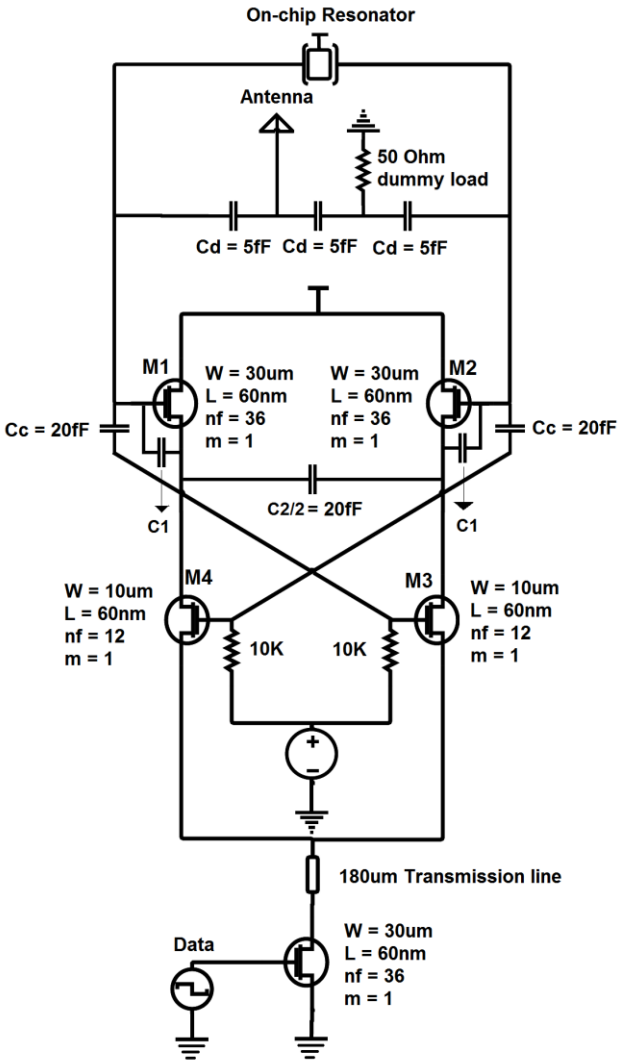


Figure 5-10 Low voltage modified Colpitts oscillator

To understand the development of this oscillator, we begin by reviewing the oscillation frequency and the startup condition of different oscillators. Upon finishing the review, the advantages of the modified Colpitts oscillator become evident.

First for the case of a simple cross-coupled VCO, the following open loop transfer function can be derived:

$$H(s) = \frac{s \times \frac{gm \times R_{tank}}{2} \times \frac{L_{tank}}{2}}{\frac{s^2 L_{tank} C_{tank} R_{tank}}{2} + \frac{s L_{tank}}{2} + \frac{R_{tank}}{2}} \tag{5.29}$$

By setting $|H(s)| = 1$, the following equations can be obtained for the oscillation frequency and the startup condition:

$$f_o = \frac{1}{2\pi\sqrt{LC}} \tag{5.30}$$

$$gm \times R_{tank} \geq 2 \tag{5.31}$$

In the case of Colpitts oscillator shown in Figure 5-11, the following open loop transfer function can be derived:

$$H(s) = \frac{s^2 gmRpL1C1}{S^3 L1RpC1C2 + S^2(L1RpC1gm + L1C2 + L1C1) + s(C2Rp + gmL1 + C1Rp) + gmRp} \tag{5.32}$$

By setting $|H(s)| = 1$, the following equations can be obtained for the oscillation frequency and the startup condition:

$$f_o \approx \frac{1}{2\pi\sqrt{\frac{L1(C1C2)}{C1 + C2}}} \text{ (for the case where Rp approaches } \infty) \tag{5.33}$$

$$gmRp \geq 4 \text{ (miumum, for the case where C1 = C2)} \tag{5.34}$$

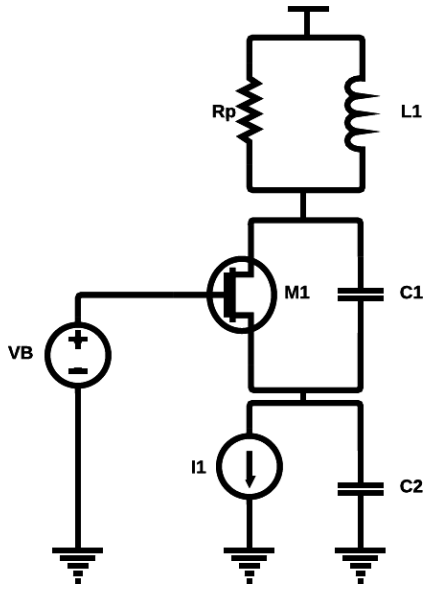


Figure 5-11 Colpitts oscillator

It can be seen that the startup condition in the case of Colpitts oscillator is more difficult to satisfy compared to the case of a simple cross-coupled oscillator. However,

the phase noise is better in case of Colpitts oscillator because the current source injects noise in the tank when the output voltage at its peak.

In the case of differential Colpitts oscillator shown in Figure 5-12, the following open loop transfer function can be derived:

$$H(s) = \frac{\frac{s^2 gmRpLC1}{4}}{\frac{S^3 LRpC1C2}{2} + S^2\left(\frac{LRp}{4}\, C1gm + \frac{L}{2C2} + \frac{L}{2C1}\right) + s\left(\frac{2C2Rp}{2} + \frac{gmL}{2} + \frac{C1Rp}{2}\right) + \frac{gmRp}{2}} \tag{5.35}$$

By setting $|H(s)| = 1$, the following equations can be obtained for the oscillation frequency and the startup condition:

$$f_o \approx \frac{1}{2\pi\sqrt{\frac{L1(C1C2)}{C1 + C2}}} \text{ (for the case where Rp approaches } \infty) \tag{5.36}$$

$$gmRp \geq 8 \text{ (miumum, for the case where } C1 = 2C2) \tag{5.37}$$

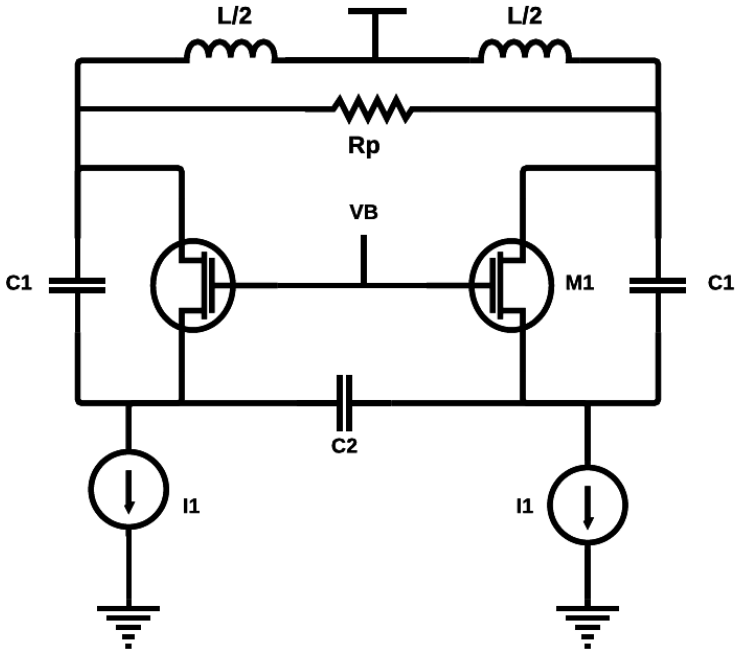


Figure 5-12 Differential Colpitts oscillator

It can be seen that the startup condition is even harder to fulfill compared to the case of single ended Colpitts oscillator.

In the case of the modified Colpitts oscillator [33] shown in Figure 5-13, the following open loop transfer function can be derived:

$$H(s) = \frac{s^2 gm1Rp\ LC1}{S^3 LRpC1C2 + S^2(L1RpC1gme + LC2 + LC1) + s(C2Rp + gmeL + C1Rp) + gmeRp} \tag{5.38}$$

Where gme = gm1 – gm2,

By setting $|H(s)| = 1$, the following equations can be obtained for the oscillation frequency and the startup condition:

$$f_o \approx \frac{1}{2\pi\sqrt{\frac{L(C1C2)}{C1 + C2}}} \text{ (for the case where Rp approaches } \infty) \tag{5.39}$$

High-frequency operation is required. For the case of C2=10C1, the following equation can be used:

$$f_o \approx \frac{1}{2\pi\sqrt{LC1}} \ (\text{C2} = 10\text{C1}) \tag{5.40}$$

In this case, the startup condition is:

$$gmRp \geq 12 \text{ (or the case where gme} \approx 0) \tag{5.41}$$

This condition is hard to fulfill.

In the opposite case where C1=10C2:

$$f_o \approx \frac{1}{2\pi\sqrt{LC2}} \ (\text{C2} = 10\text{C1}) \tag{5.42}$$

In this case, the startup condition is:

$$gmRp \geq \frac{12}{11} \text{ (for the case where gme} \approx 0) \tag{5.43}$$

In this case, this oscillator has a more relaxed startup condition compared to the cross-coupled oscillator. However, the minimum supply voltage required for operation is $2V_{gs} + V_{DS,sat}$.

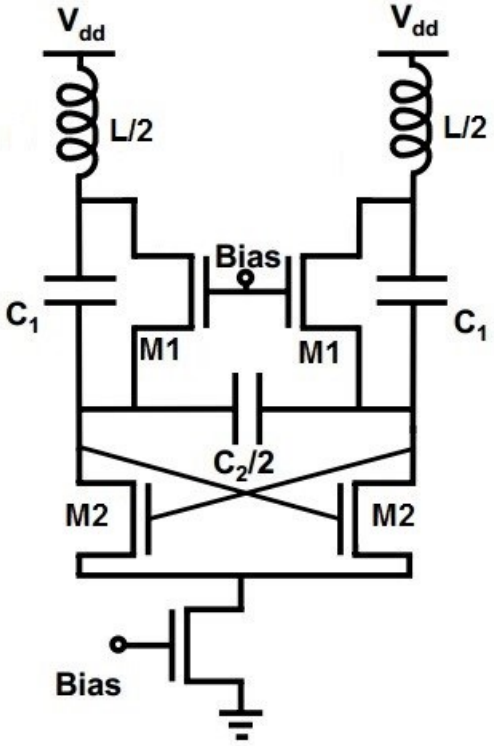


Figure 5-13 Oscillator proposed in [33]

Finally, the startup condition and the frequency of oscillation is determined for the case of the proposed oscillator. Figure 5-14 show the half circuit of the proposed oscillator that was used to derive the oscillation open loop transfer function. Here a few assumptions are made to simplify the derivation: The capacitance Cc is assumed to be very large, and the resonator is replaced by an inductor and resistance to model losses, and the transconductance of both transistors is assumed to be equal. Moreover, the oscillator is assumed to be unloaded. The following transfer function can be derived:

$$H(s) = \frac{s^2 gm1Rp\ LC1}{\frac{S^3 LRpC1C2}{2} + S^2(LC2 + LC1) + s(C2Rp + gmL + C1Rp) + gmRp} \tag{5.44}$$

From this open loop transfer function, the following two equations can be derived for the oscillation frequency and the startup condition:

$$f_o \approx \frac{1}{2\pi\sqrt{\frac{L}{2}\frac{(C1C2)}{C1 + C2}}} \text{ (for the case where Rp approaches } \infty) \tag{5.45}$$

$$gmRp > \frac{4 + 2(\frac{C1}{C2} + \frac{C2}{C1})}{2 + \frac{C2}{C1}} \tag{5.46}$$

High-frequency operation is required. For the case of C2=10C1, the following equation can be used:

$$f_o \approx \frac{1}{2\pi\sqrt{\frac{L}{2}C1}} \ (\mathrm{C2} = 10\mathrm{C1}) \tag{5.47}$$

In this case, the startup condition is:

$$gmRp \geq 2.01666 \tag{5.48}$$

This condition is very similar to the case of cross-coupled oscillator.

In the opposite case where C1=10C2:

$$f_o \approx \frac{1}{2\pi\sqrt{\frac{L}{2}C2}} \ (\mathrm{C2} = 10\mathrm{C1}) \tag{5.49}$$

In this case, the startup condition is:

$$gmRp \geq 11.5238 \tag{5.50}$$

This condition is hard to fulfill.

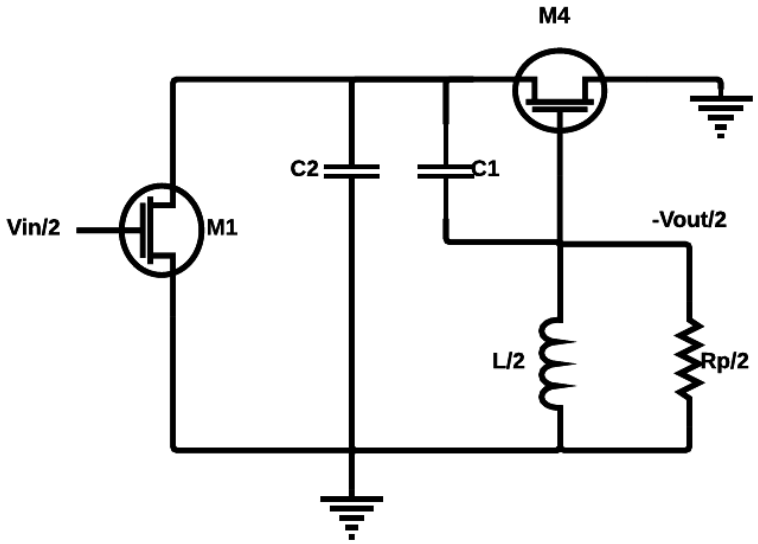


Figure 5-14 Half circuit of the proposed oscillator.

It can be seen that the startup condition can be similar to the case of a cross-coupled oscillator. Moreover, compared to the case of the modified Colpitts oscillator proposed in [33], this design can operate at lower supply voltages: $V_{gs}+ V_{DS,sat}$. Also, since the supply voltage node is separated from the resonator node, the supply voltage common mode node can be used to extract the second harmonic, thus, building an oscillator capable of operating at twice the differential model operating frequency. Finally, the oscillation frequency is determined by the smallest capacitor leading to higher oscillation frequency as seen by equations 5.47 and 5.49.

The phase noise is also good in this oscillator because the current flows in the transistor when the output voltage at its peak.

5.5 Simulation results

The response of the first oscillator, Figure 5-4, is shown in Figure 5-15. The start-up time is around 3ns. The output power -2dBm, with a power consumption of 3.3mW.

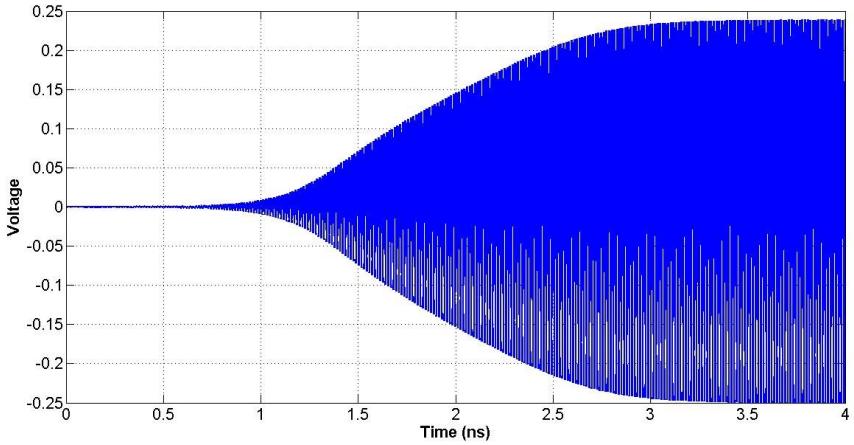


Figure 5-15 Start-up of 1st oscillator

The response of the second oscillator, Figure 5-10, is shown in Figure 5-16. The start-up time is around 1.5ns. The output power 2dBm, with a power consumption of 5mW.

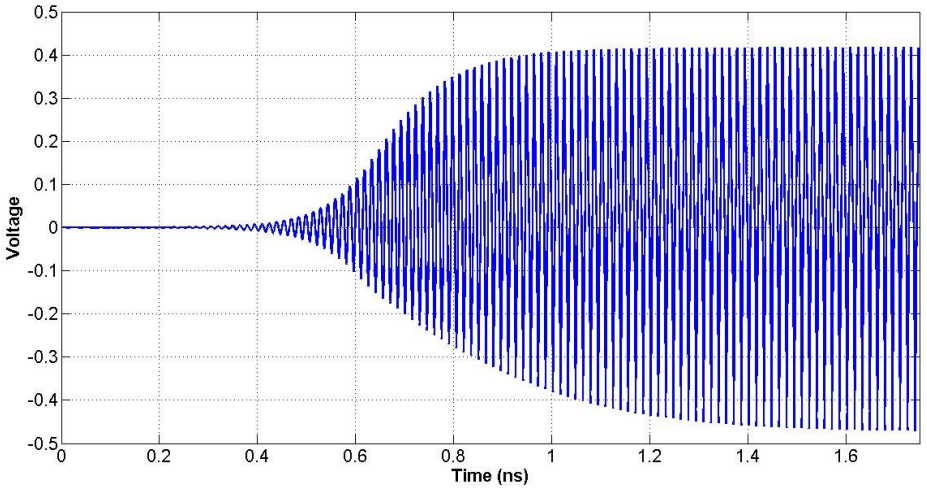


Figure 5-16 Start-up of 2nd oscillator

Both oscillators exhibit a similar phase noise of -90dBc/Hz @ 1MHz offset and -117dBc/Hz @ 10MHz offset.

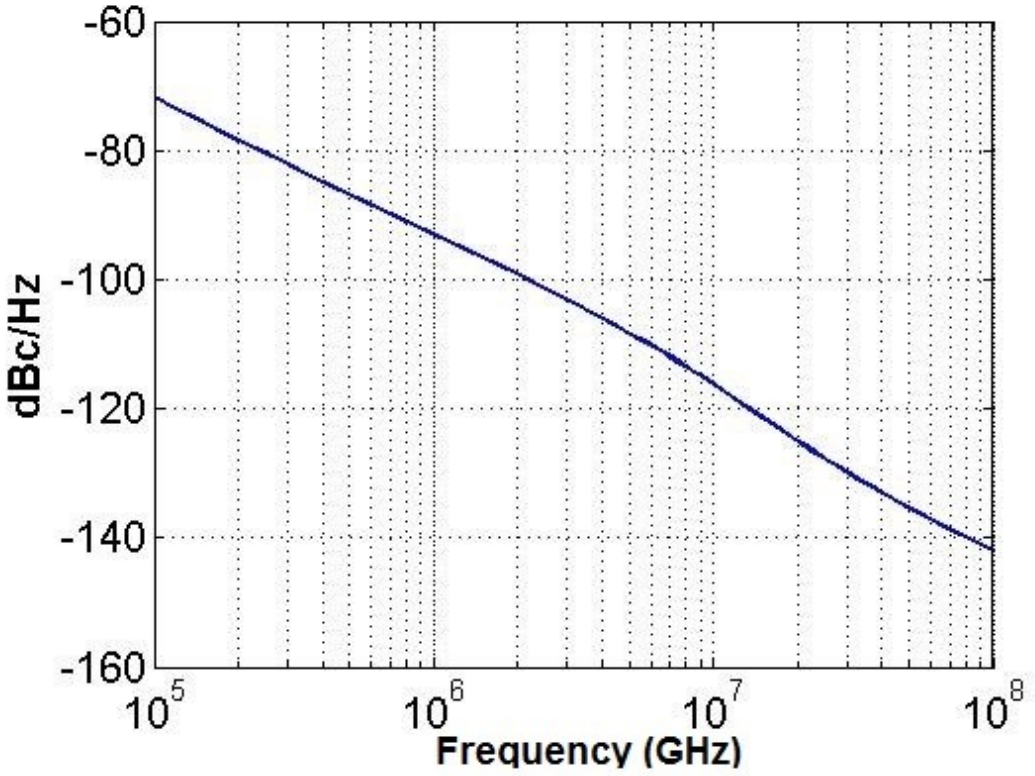


Figure 5-17 Phase noise of both oscillators

Summary of simulations is shown next:

Specification	Oscillator 1	Oscillator 2
Frequency	72.56	64GHz
Output power	-2dbm	2dbm
Phase noise	90dBc/Hz @ 1MHz offset -117dBc/Hz @ 10MHz offset.	90dBc/Hz @ 1MHz offset -117dBc/Hz @ 10MHz offset.
Startup time	3ns	1.5ns
Power consumption	3.3mW	5mW

CHAPTER 6

The design of an all-digital Phase Locked Loop (ADPLL)

6.1 Introduction

A phase-locked loop (PLL) is an important building block of a modern communication systems. Although, the application space is dominated by analog implementations, digital PLL's are used for low-end applications where jitter requirements are not very demanding (e.g. clock generation in microprocessors, on-chip communication between microprocessor and memory or microprocessor to microprocessor in a multi-core Systems On Chips (SoCs)). Charge pump PLL's with passive loop filters have the best performance, but the real estate required for the implementation of the filter renders them an expensive solution. Digital PLL's occupy less area than their analog counterparts and are perfectly suited for many SoC application in the wireless transceiver proposed in this work, the data rate is low (100KB/s). Hence, the jitter of the PLL is not very stringent. This chapter is related to the implementation of the novel all-digital PLL with a very short pull-in time. An important feature is its large capture range limited only by the tuning range of the VCO (of a ring type). The advantage of this implementation can be understood when configuring the PLL in a Data and Clock Recovery (DCR) system with random data. As long as the frequency of the data is within the capture range of the PLL, the pull-in time is very short, in the order of μs and there is no need for and external crystal oscillator to keep the ring voltage controled oscillator frequency

close to the frequency of the incoming data. A possible use of the digital PLL is shown in Figure 6-1, where the clock input of the digital PLL is a divided version of the oscillator clock output. The On-Off keying (OOK) data are used to modulate the output of the digital PLL, which in turn is used to turn on/off the Power Amplifier (PA) or Buffer.

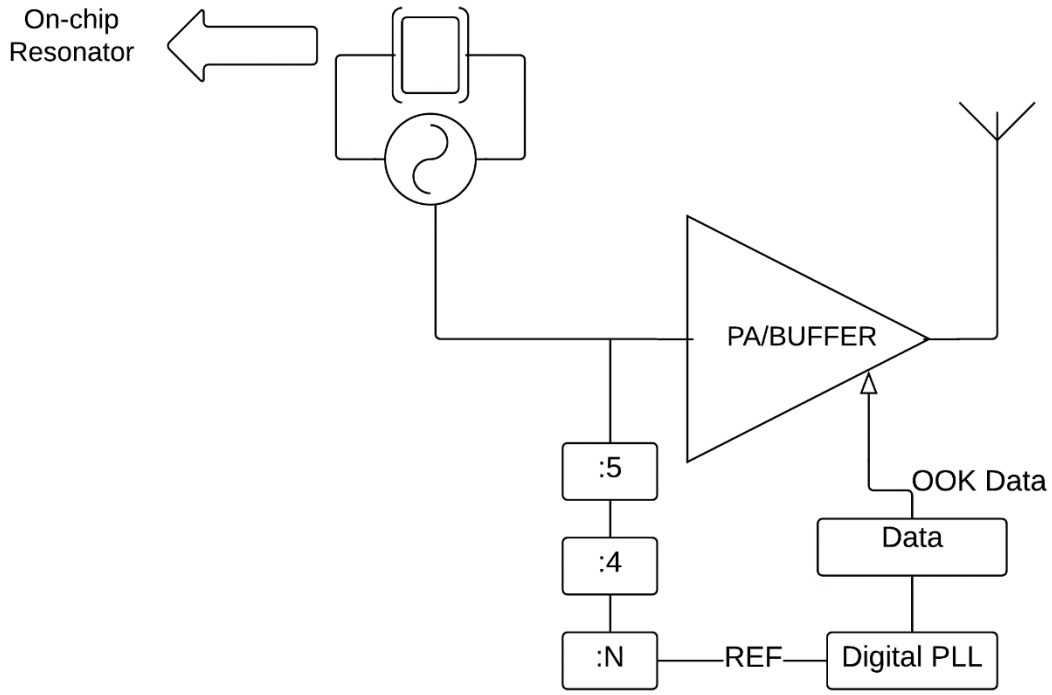


Figure 6-1 Possible use of digital PLL

This chapter begins with a review of the state of the art digital PLLs, the system block diagram, followed by the implementation of the frequency detector, the phase detector, and the digitally controlled oscillator.

6.2 Specifications

Since the transmitter is capable of operating in a very wide range of data rates, where the fastest data rate is only limited by the start-up time of oscillator and data pulse width that the receiver is capable of demodulating, and there is no limit on the slowest data rate, a PLL capable of operating in a wider range of frequencies is required.

For this reason, **a frequency operating range between 10MHz and 100MHz will be targeted**. Moreover, to reduce transient power consumption, a very fast pull-in is required. Hence, we set a **pull-in time of less than 10μs**. Finally, a **power consumption of less than 100 μW** of an **all-digital implementation** is targeted. An all-digital implementation is targeted since it can be used in many applications conveniently.

A summary of the specification is shown below for the all-digital phase-locked loop:

- An output frequency operating range between 10MHz and 100MHz will be targeted
- A pull-in time of less than 10μs
- A power consumption of less than 100 μW.
- An all-digital implementation

6.3 Survey

A1.25 GHz all-digital phase-locked loop with supply noise suppression is presented in [34]. This design utilizes a bang-bang type phase frequency detector and a first order digital loop filter to generate the control signals needed to tune the frequency of the digitally controlled oscillator (DCO). Fine tuning is achieved by using a 5-bit delta sigma modulator while the thirty thermometer bits of the digital loop filter are used control varactors in the DCO in order to implement coarse tuning. The DCO consists of a tetrahedral oscillator and digitally controlled PMOS varactors. Moreover, this design utilizes an adaptive bandwidth circuit in order suppress jitter

when supply noise is present, and a fast locked circuit in order to speed up locking time. A performance summary and comparison is provided in the table below. Notably, this design consumes a power consumption of 9mW and requires a reference clock.

In [35], a 4-to-10.5Gb/s clock and data recovery circuit is presented. Similar to the previous design, this circuit employs a bang-bang phase detector that provides early and late (E/L) signals to update a frequency and delay - phase-locked loops. Moreover, the digitally controlled oscillator implemented in this design is implemented using a fractional-N phase-locked loop employing a single ring oscillator instead of multiple LC oscillators. However, this design requires a charge pump in its DCO implementation in addition to requiring a reference clock of 50MHz. A Performance summary is provided in the table below.

In [36], a 0.4-to-3GHz digital phase locked loop is presented. This design utilizes a proportional and integral paths to achieve frequency control. While the phase locked loop is digital, the digitally controlled oscillator, however, contains a digital to analog converters. The digitally controlled oscillator in this design is a ring oscillator. Although the concept of using a proportional and integral paths to achieve frequency control is known in the literature, this design provides a supply noise cancelation technique. A Performance summary is given in the table below.

A recent implementation of a fully integrated fractional-N PLL based on a second order frequency-to-digital (FDC) converter is presented in [37], which is an extension of the architecture proposed in [38]. A Performance summary is provided in the table below.

Table 6-1 Survey Summary

Design	Process	Supply	Reference frequency	Output frequency/ Data rate	RMS jitter	Pk-Pk jitter	Power consumption	Core area
[34]	0.18um CMOS	1.8	39.0625 MHz	1.25GHz	0.58907ps 7.37ms UI	38.9ps 0.049 UI	9mW	0.348 $\boldsymbol{mm^2}$
[35]	65nm	1.2/1.0	50MHz	4-10.5Gb/s	2.2ps	4ps	22.5mW @10Gb/s	1.63 $\boldsymbol{mm^2}$
[36]	0.13um CMOS	1	-	0.4 – 3 GHz	5ps	46ps	3.4mW	0.08 $\boldsymbol{mm^2}$
[37]	65nm	1.0/1.2	26MHz	3.5GHz	-	-	21mW	0.56 $\boldsymbol{mm^2}$

6.4 System block diagram

The oscillation for the Tx function is turned ON/OFF with the OOK data. In order to generate data, the clock is synthesized from the digital PLL. The block diagram of the implemented PLL is shown in Figure 6-2.

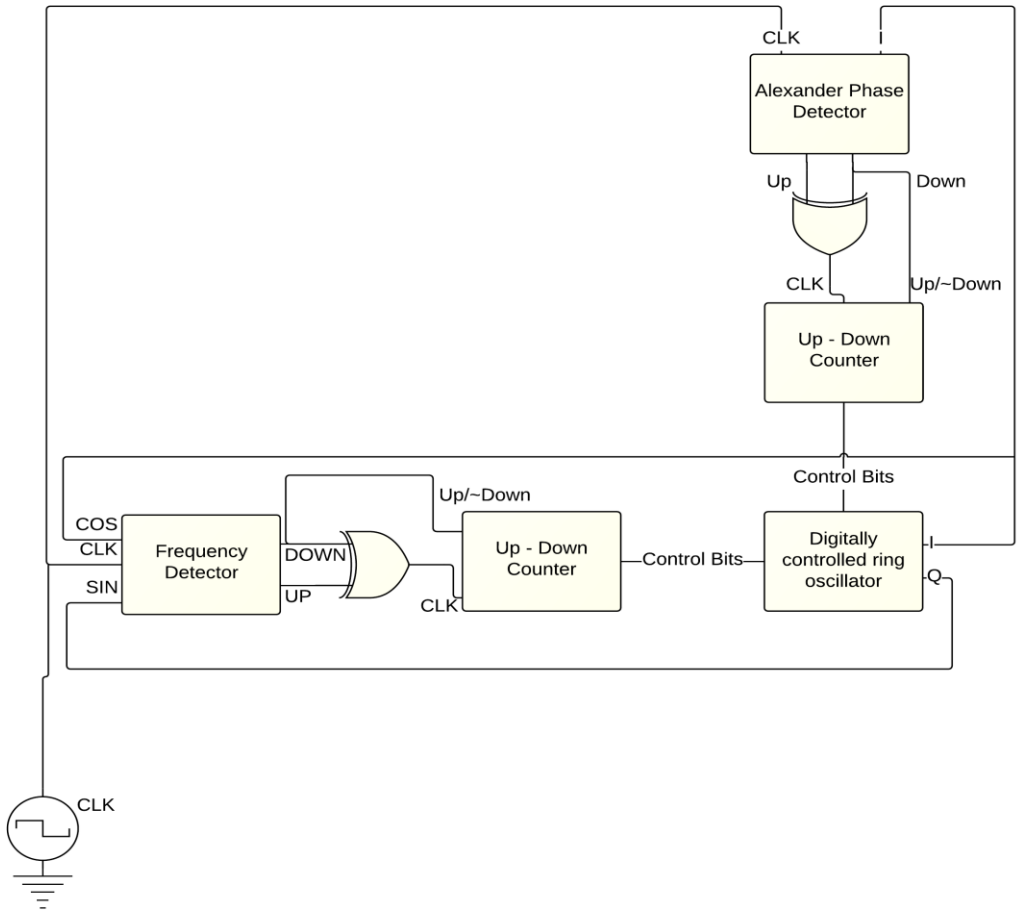


Figure 6-2 All digital PLL block diagram

In this PLL, the frequency detector compares the frequency of the incoming clock and the frequency of the local clock and produces pulses, either on the UP or DOWN signals, depending on which frequency is higher. That is, if the frequency of the local clock is higher than the frequency of the incoming clock, a pulse on the HIGH signal is produced, and if the frequency of the local clock is lower than the frequency of the incoming clock, a pulse on the LOW signal is produced.

An integrator is needed to produce an output that is promotional to the error between the incoming clock and the local clock. To completely digitize the design, this integrator will be implemented using an up-down counter – replacing the charge pump of the analog counterpart.

the LOW signal sets the counting direction; if the LOW signal is high, then that means that the local clock frequency is lower than the frequency of the incoming signal and the number stored in the counter will increase. The exact opposite happens when the HIGH signal is high.

The XOR gate is used to connect both signals, HIGH and LOW, to the input of the synchronous counter.

Alexander phase detector was utilized in a similar fashion to the frequency detector.

The digitally controlled ring oscillator is controlled by the outputs of the two up-down counters and produces two quadrature clock signals at the same frequency of that of the incoming clock.

6.5 Frequency detector

The frequency detector implemented was based on the design found in [39]. A block diagram is shown Figure 6-3.

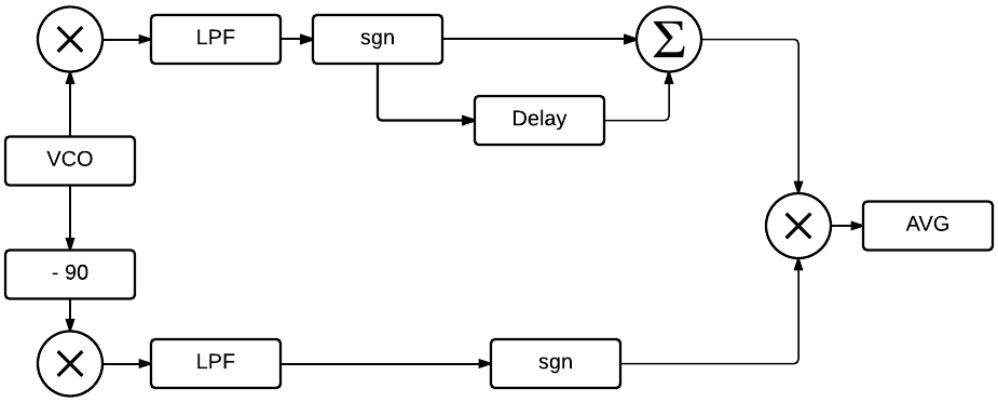


Figure 6-3 Block Daigram of digital Quadricorrelator

The final output of this circuit is in the form of

$$Vd(t) = K_F\,\Delta\omega \tag{6.1}$$

Where

$$K_F = 2\,\frac{Delay}{\pi}\,. \tag{6.2}$$

This means that the output follows the magnitude and the sign of the frequency difference between the local clock and the incoming signal. This error can be used to adjust the frequency of the VCO in order to obtain the correct frequency.

Figure 6-4 shows the implementation of the digital quadricorrelator. In this implementation, the mixers and the low pass filters are implemented using two flip-flops where the incoming clock is used as the D input and the quadrature clocks are used the clock inputs. Moreover, the third flip-flop and the two following AND gates are used to implement the differentiator. Finally, the last four AND gates and the two OR gates, are used to implement the cross-correlator and the summer, respectively.

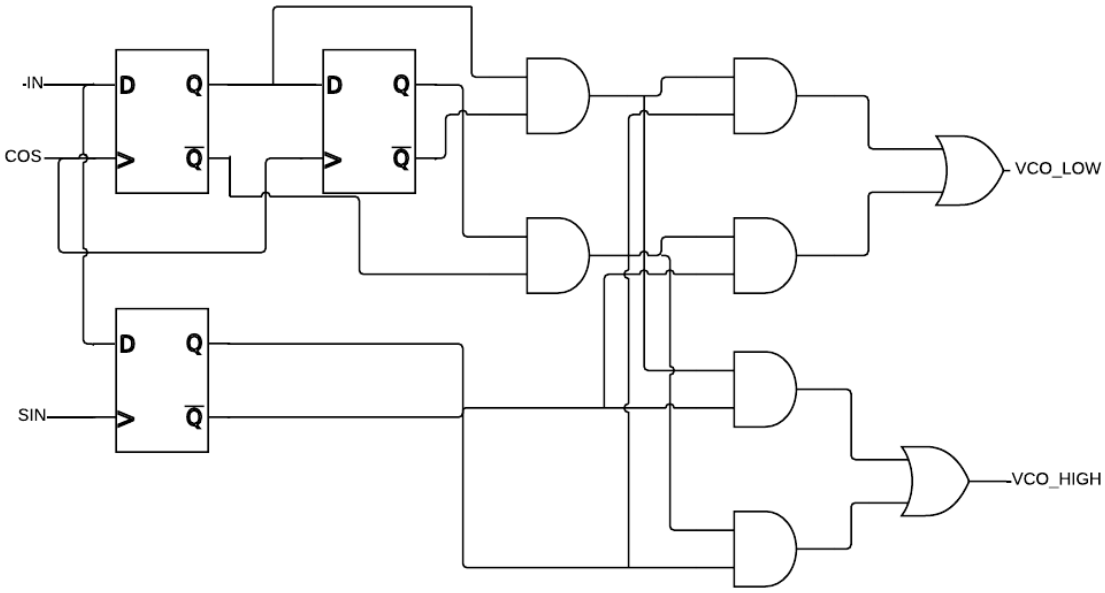


Figure 6-4 Implementation of digital quadricorrelator

Simulation of this implementation resulted in a frequency discrimination range of less than 15%. Hence, it is not possible to use this implementation in designs requiring operation over a broad range of frequencies. This design can be modified in order to extend the discrimination range.

Figure 6-5 shows the modified implementation that is a modified version of the design found in [39]. This circuit utilizes a broad range multiplier, shown in Figure 6-6, which replaces the flip-flops used to implement the mixers and the low pass filters. The flip-flop used in the implementation of the differentiator is used now replaced by time delay. The eight AND gates followed by two sets of three OR gates are used to generate the VCO_LOW and VCO_HIGH signals. Finally, a delay element is used to create an intentional glitch to make the VCO_LOW pulse wider than the VCO_HGIH pulse. This glitch is used to exploit the nature of the output, creating a very wide range frequency detector as will be explained later.

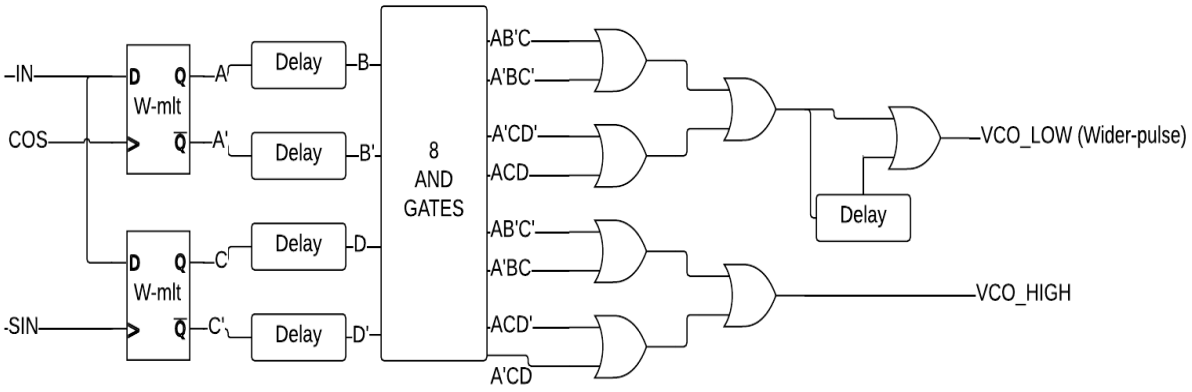


Figure 6-5 Implementation of wide range digital quadricorrelator

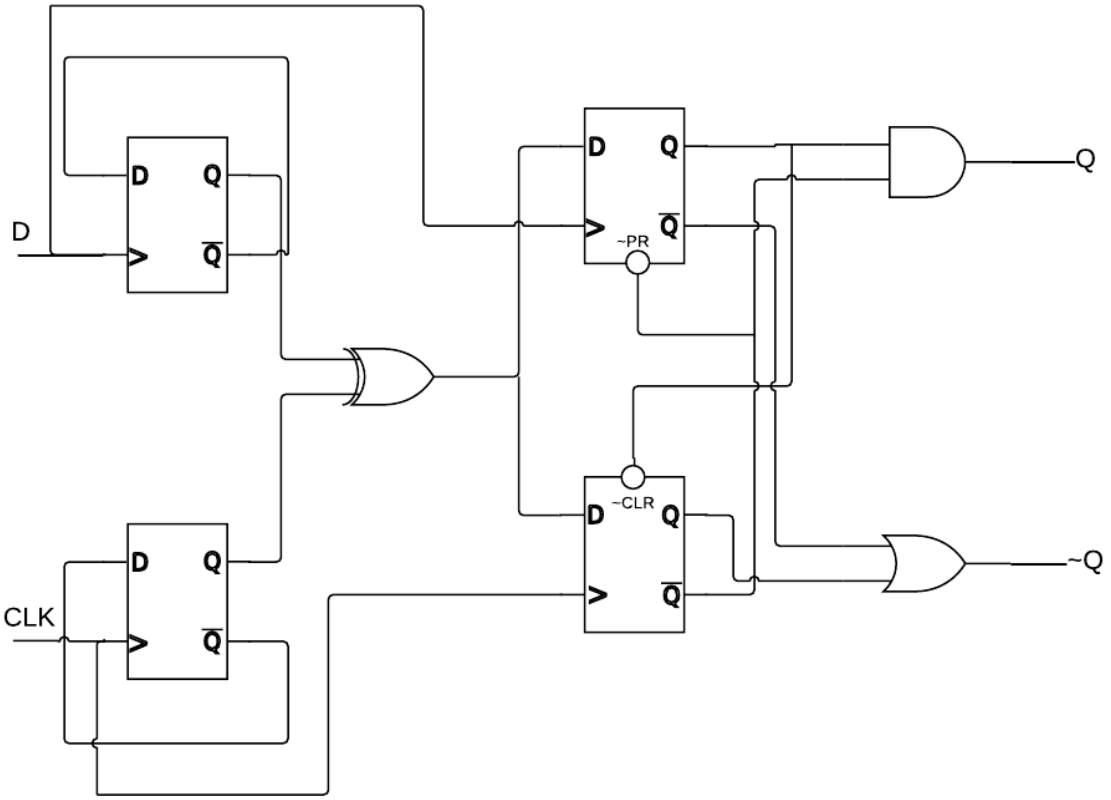


Figure 6-6 Wide range multiplier

Figure 6-7 shows the output of the frequency detector when the frequency of the local digitally controlled oscillator is lower than the frequency of the incoming signal. In this case, the VCO HIGH remains at zero, while VCO LOW pulses. In the case when the frequency of the local digitally controlled oscillator is higher than the

frequency of the incoming signal, VCO HIGH pulses while VCO LOW remains at approximately zero. The latter case is shown in Figure 6-8.

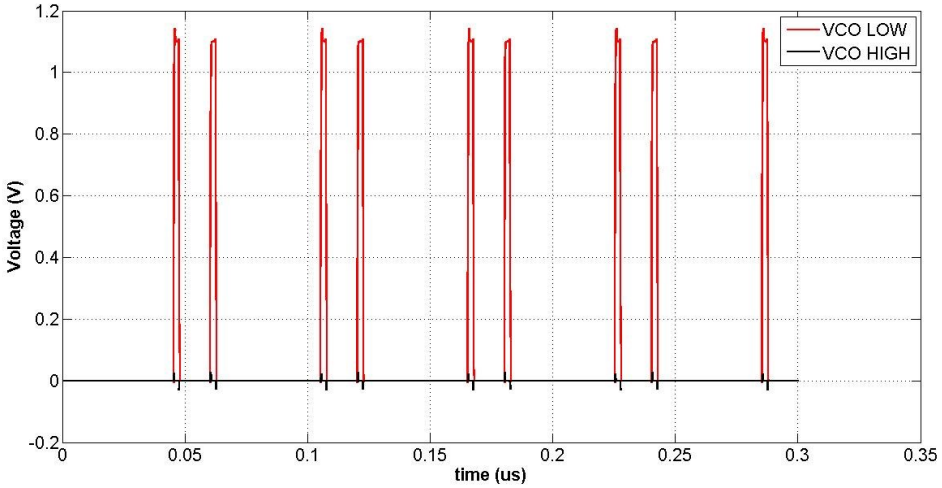


Figure 6-7 Output of the frequency detector when the local frequency is lower than the incoming clock frequency

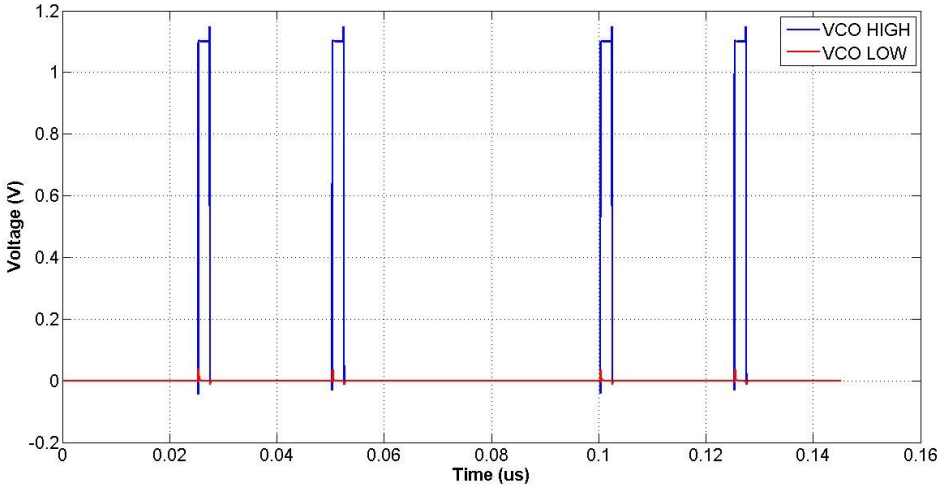


Figure 6-8 Output of the frequency detector when the local frequency is higher than the incoming clock frequency

When the input clock is at much higher or much lower frequency than the local frequency, then design presented [39] will produce overlapping VCO LOW and VCO HIGH pulses, and that causes both pulses to cancel when the XOR operation is performed. The intentional glitch makes the VCO LOW wider than VCO HIGH. This case is shown in Figure 6-9.

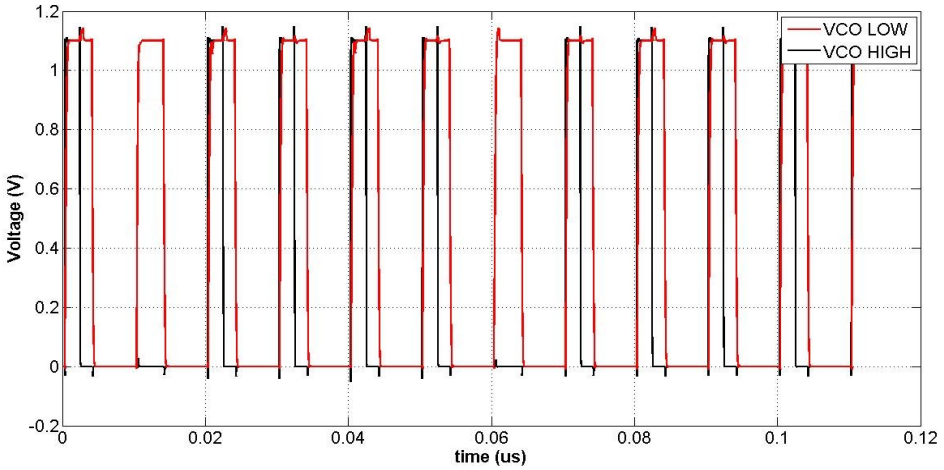


Figure 6-9 Output when the input at a much higher or a much lower frequency

When the waveforms in Figure 6-9 is an input to the XOR gate, VCO LOW is no longer completely canceled and a part of it can be seen at the output. From the point of view of the up-down counter, the counter count will increase and thus increasing the frequency of the local digitally controlled oscillator. There are two cases to consider here:

- The incoming signal is at a higher frequency and out of range: since VCO LOW is longer, the counter will increase and the frequency of the local digitally controlled oscillator will increase. This means that correct operation is ensured.
- The incoming signal is at a lower frequency and out of range: since VCO_LOW is longer, the counter will increase and the frequency of the local digitally controlled oscillator will increase. While this may look as an incorrect operation, it will eventually lock at the correct frequency: the number stored in the counter will keep increasing, and an overflow will occur, and that causes the frequency of the local digitally controlled oscillator to be minimum and then increase and lock to the correct frequency.

This means that even when the incoming clock frequency is out of the discrimination range of the original design, the modified design can still lock on the correct frequency. In terms of frequency range, the bottleneck of the system is the local digitally controlled oscillator.

Another implementation, which is shown in Figure 6-10, is a linear frequency detector based on the design proposed in [40]. The inputs to this frequency detector are two quadrature clock signals and the data clock. The outputs of this frequency detector are two error signals, UP, and DOWN, which are proportional to the polarity and the magnitude of the frequency difference between data clock and the local clock. This implementation was simulated in all three conditions: data clock is faster, slower, and in lock with the local clock. For the case where the two clocks are in sync, the output is shown in Figure 6-11. It is clear the UP, and DOWN signals have equal widths. This means that steady state is reached, which is correct, since data and local clocks are in-phase.

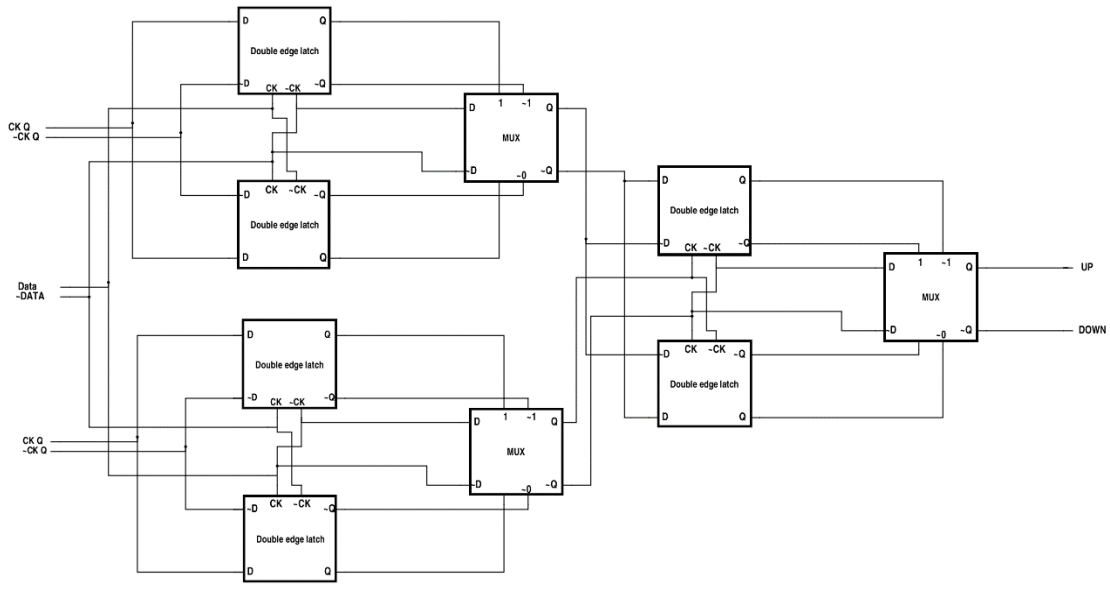


Figure 6-10 linear Frequency detector

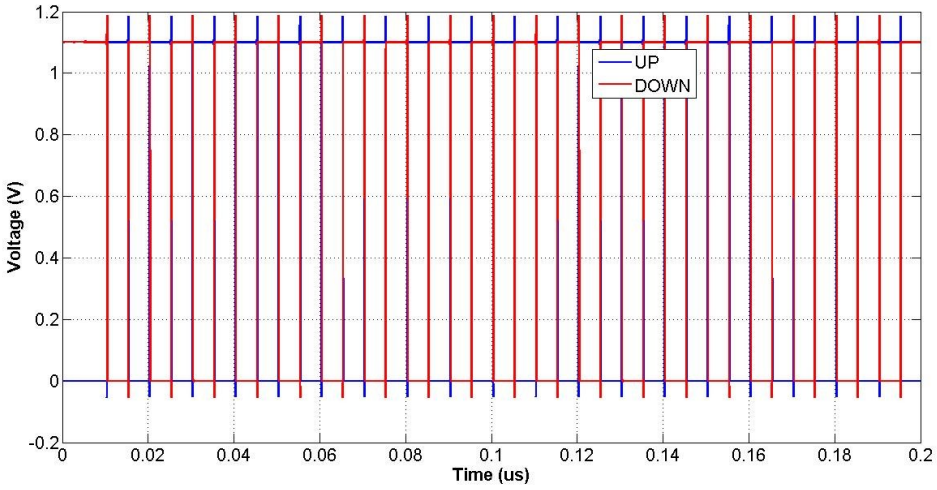


Figure 6-11 Linear frequency detector in lock

In the case where the local clock is running at a lower frequency than the incoming data clock, the waveforms are shown in Figure 6-12. DOWN signal pulse is wider than the UP signal. On the other hand, when the local clock is running at a higher frequency than the incoming data clock, the waveforms are shown in Figure 6-13.

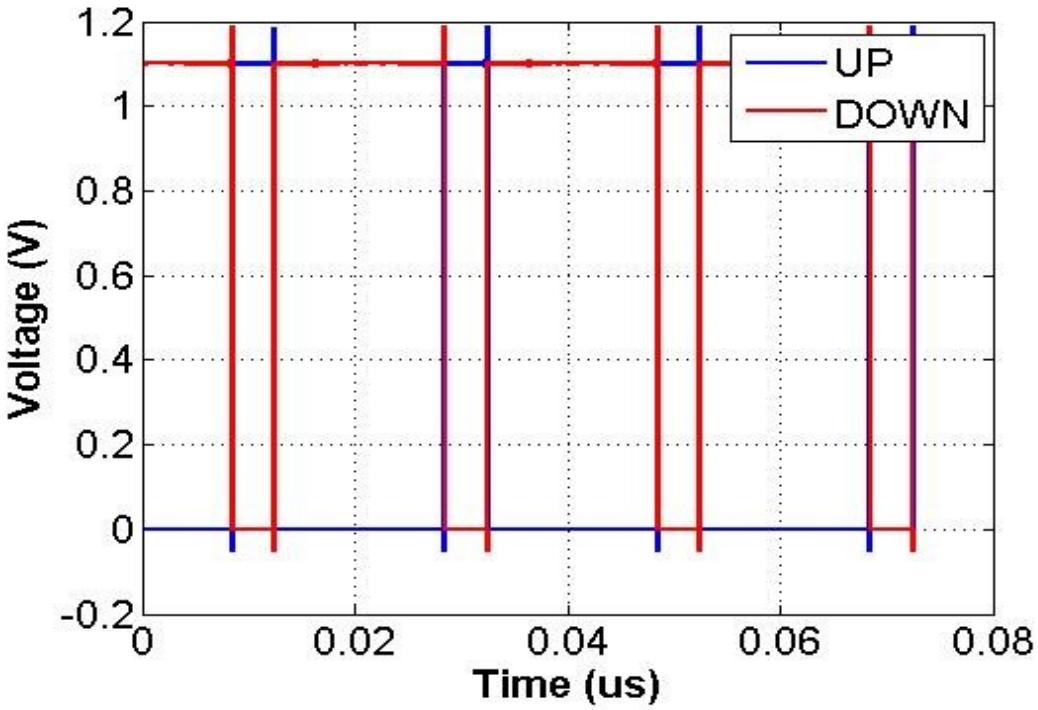


Figure 6-12 Linear frequency detector when data clock is faster than local clock

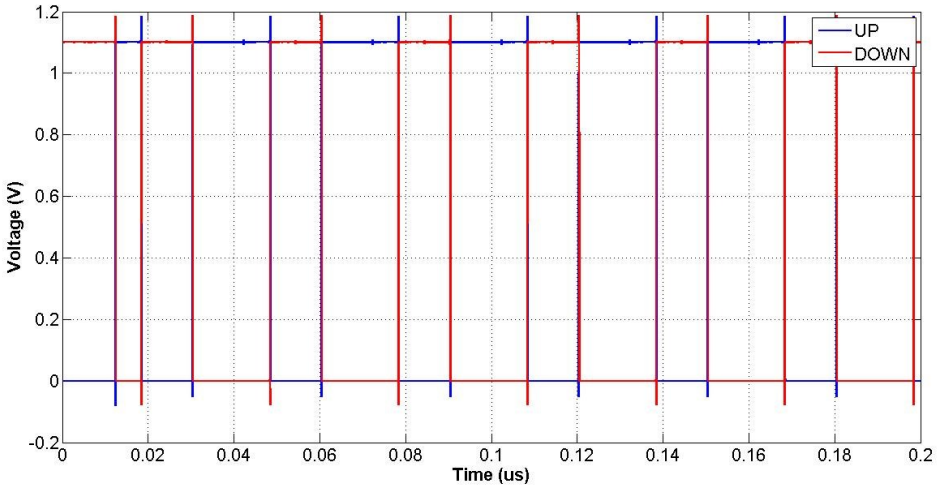


Figure 6-13 Linear frequency detector when data clock is slower than local clock

Next, the operation of the phase detector is explained.

6.6 Phase detector

Alexander phase detector was used because its output waveforms can be used directly with XOR gate and an up-down counter in a similar fashion to that of the frequency detector. Alexander phase detector is shown in Figure 6-14. The waveforms when the clock is early are shown in Figure 6-15. In this case, a pulse can be seen at the output of the DOWN signal, while the UP signal remains at zero, which is very similar to the VCO LOW and VCO HIGH pulses observed at the output of the frequency detector.

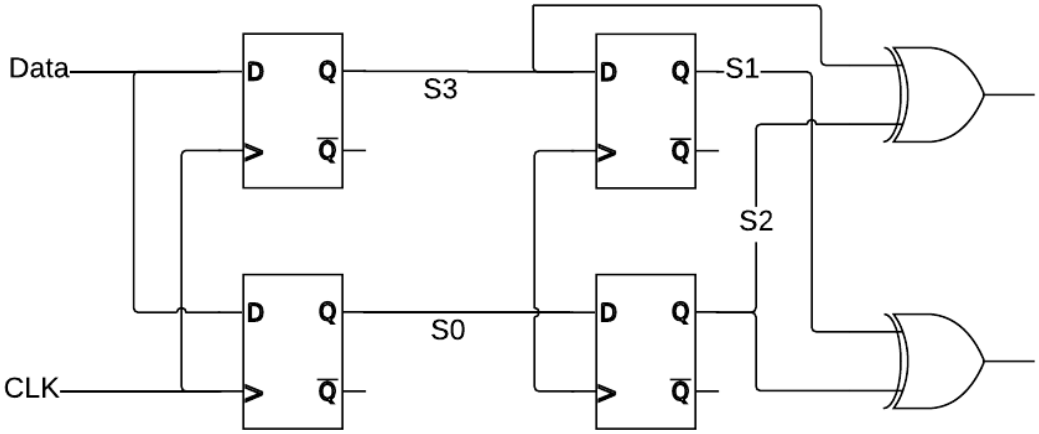


Figure 6-14 Alexander phase detector

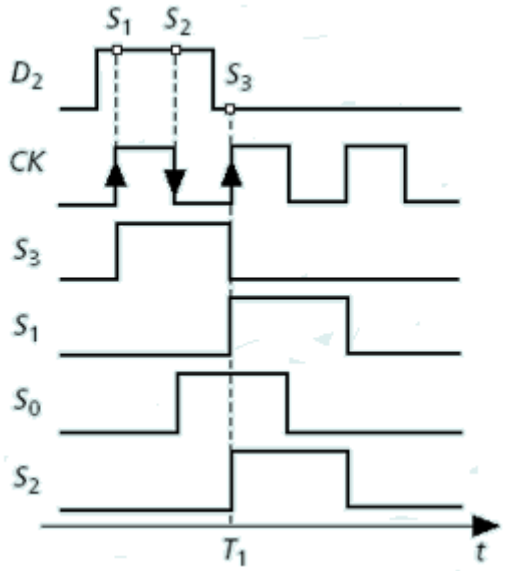


Figure 6-15Alexander phase detector waveforms when the clock is early

While Alexander phase detector is a bang-bang type of a phase detector, there are some advantages in using it over other types of phase detectors: its output can be used in a digital way, unlike linear types of phase detectors that need a charge pump, its output is self-aligned, and it generates a zero when there are no transitions.

Other implementations such as Hogge phase detector were also simulated. While exhibiting linear characteristics, it is not possible to use it in a pure digital implementation because of its output being two pulse width modulated, UP and

DOWN, signals with a width proportional to the error magnitude and direction. This means that a charge pump is needed to process these signal instead of an up-down counter.

Another implementation that is similar to Hogge phase detector in terms of output waveforms is shown in Figure 6-16. In this implementation, the inputs are two quadrature clocks, Vb and Va, and the data clock. The outputs of this implementation are two signals, Up, and Down, which represent a pulse width modulated error signal proportional to the polarity and the magnitude of the frequency difference.

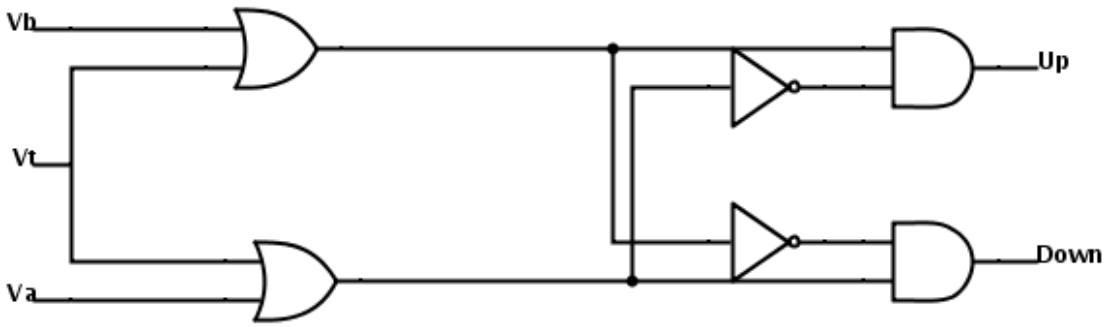


Figure 6-16 Linear phase detector

To better understand the outputs of this circuit, it was simulated with data clock and the local clock in-phase. The output waveform, in this case, is shown in Figure 6-17. In this case, the Down signal is always pulsing, which means that even though clocks are synchronized, there is still an error signal.

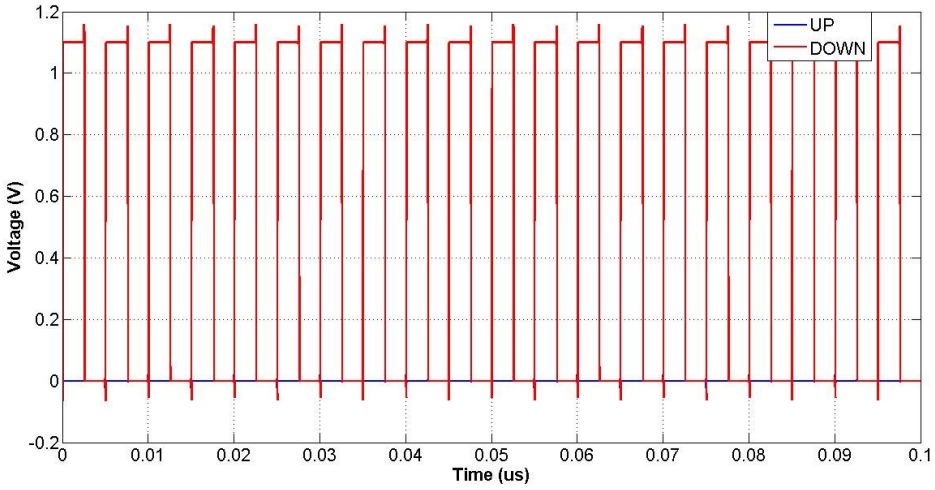


Figure 6-17 Linear phase detector output waveforms when in-phase data and local clocks

The other extreme is having quadrature data and local clocks. Again, the simulation shows that the Up signal is always pulsing as shown in Figure 6-18. Finally, having the data and local clocks 1/8th clock cycle, or 22.5 degrees, out of phase produces the waveform shown in Figure 6-19. If the output were to be connected to a charge pump, then this would be the steady state condition of the circuit. Although the output is digital, the circuit cannot be used in conjunction with an up-down counter because of the nature of the pulse width modulated outputs.

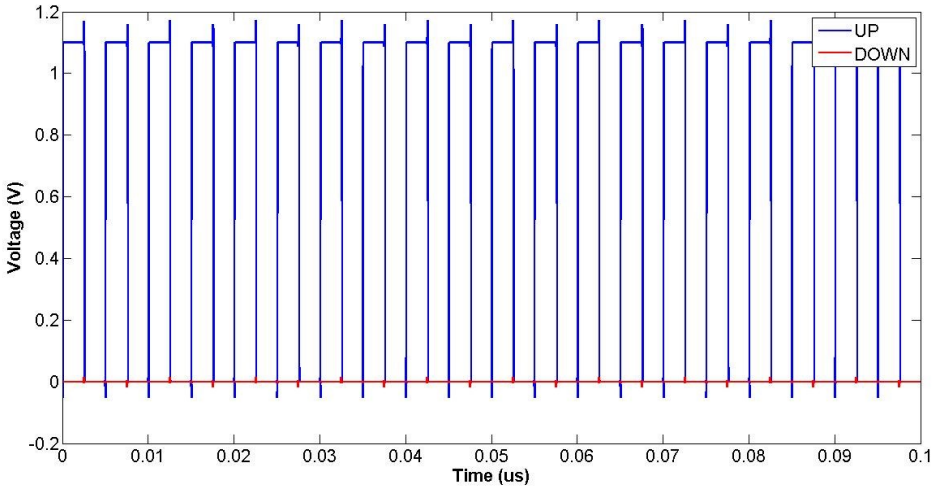


Figure 6-18 Linear phase detector output waveforms when quadrature data and local clocks

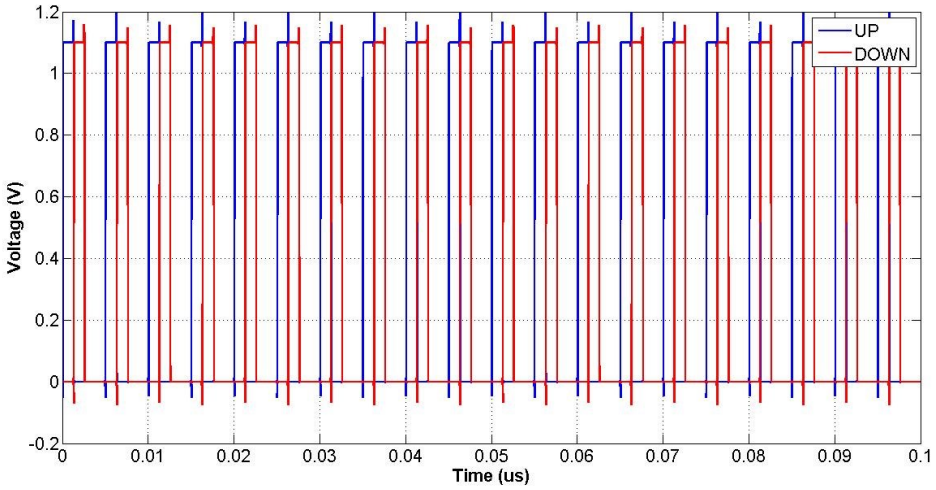


Figure 6-19 Linear phase detector output waveforms when data and local clocks are 22.5 degrees out of phase

6.7 The Up-Down Counter

A schematic of the 3 bits up-down counter is shown in Figure 6-20. The number of bits could be increased to obtain finer frequency control over the range of operation. This design is based on JK flip-flops and the control signal, UP/~DOWN, is controlled through the DOWN control signal coming from the frequency and phase detectors. If the DOWN signal is high, then the counter counts in the up direction, and the frequency/phase is increased. Thus, a negative feedback is achieved.

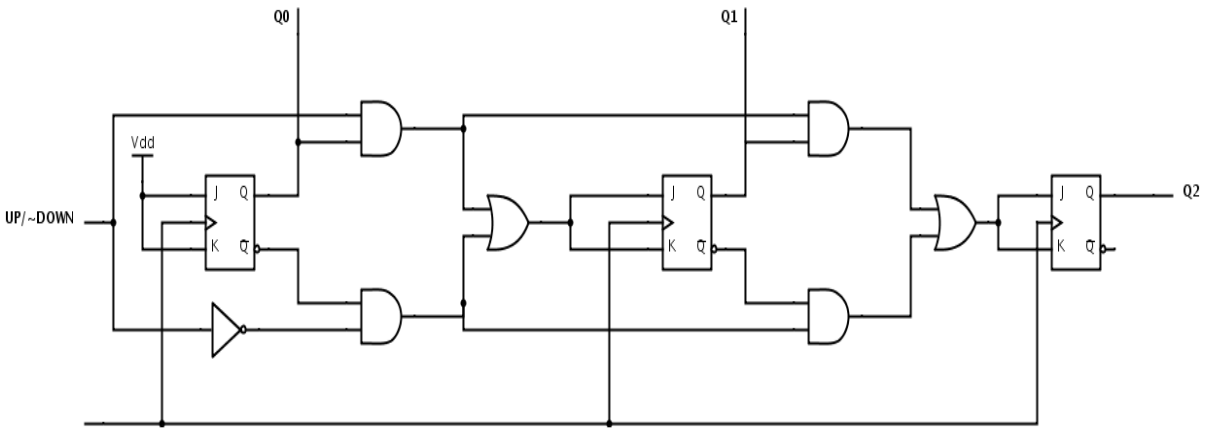


Figure 6-20 up-down counter

6.8 Digitally controlled oscillator

Shown in Figure 6-21 is a simplified schematic of the digitally controlled oscillator. The oscillator is made of two cross-coupled sets of four inverters. This topology allows for obtaining four quadrature single-ended and differential clock signals. The back to back inverters ensure that rise and fall times are equal. Frequency and phase are controlled using output bits coming from the output of the two up-down counters.

Frequency control is accomplished using one of four methods:

i. Control bits can be used to control PMOS transistors acting as current sources. The response of the technique is finer at higher frequencies and can be used when most incoming signals are coming at high frequencies. In this method, each bit can turn on/off a number of current sources corresponding to its weight. For example, the third least significant bit (Bit 2) controls four current sources, since $2^2 = 4$. Control bits coming from the up-down counter corresponding to the phase detector, control scaled PMOS transistors in a way to make them weaker than the PMOS transistors controlled by the up-down counter corresponding to the frequency detector. Frequency vs. frequency counter count for this case is shown in Figure 6-22.

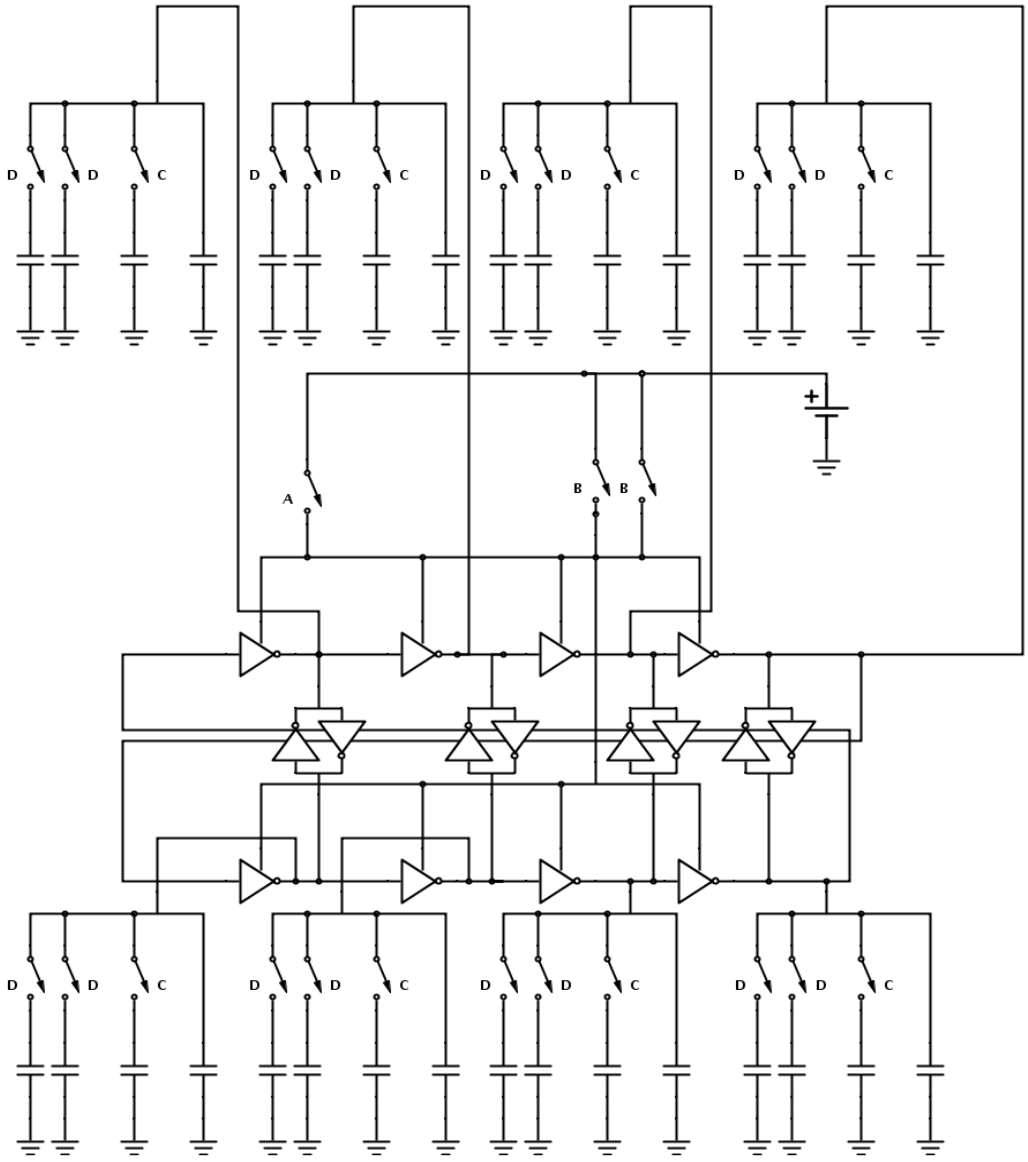


Figure 6-21 simplified schematic of the digitally controlled oscillator

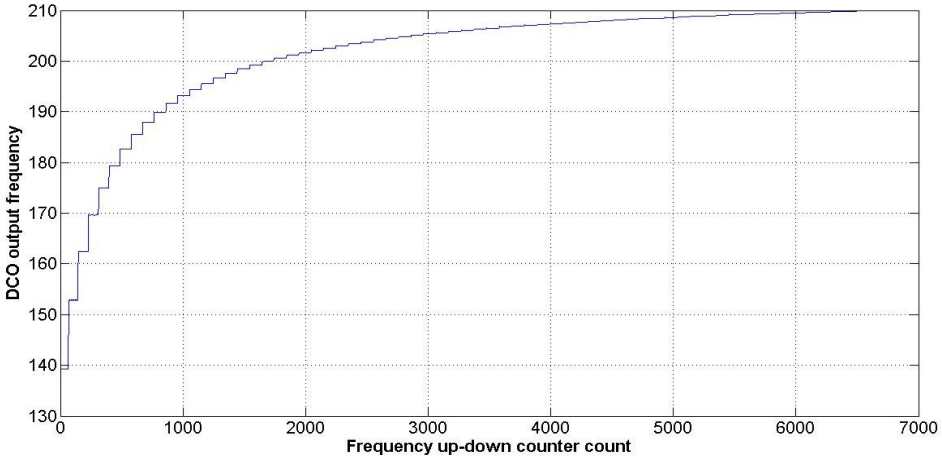


Figure 6-22 frequency vs. frequency up-down counter count – case i

ii. Control bits can be used to control PMOS transistors acting as a switch connected to load capacitors. Turning on a switch caused the circuit to "see" the capacitor as a load and the frequency decreases. Control bits are used in the same fashion stated in the first technique. The response of the technique is finer at lower frequencies and can be used when most incoming signals are coming at low frequencies. Frequency vs. frequency counter count for this case is shown in Figure 6-23

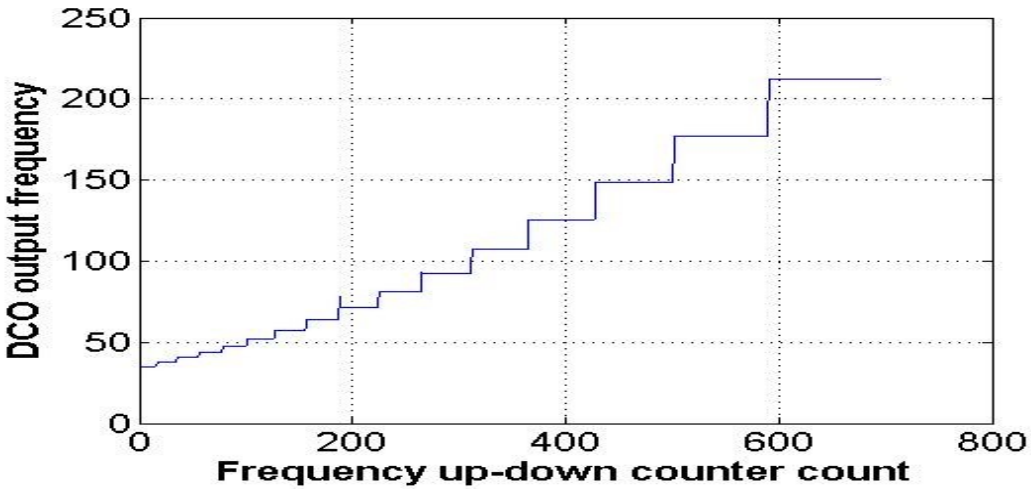


Figure 6-23 frequency vs. frequency up-down counter count – case ii

iii. A combination of both techniques above can be used. The most significant bits can control capacitors while least significant bits can control current sources or vice versa. This requires careful sizing of capacitors and current sources to ensure that loads are consistent with the weight of the control bit. For instance, if the most significant bits set is used to control capacitors and the least significant bits set is used to control current sources, then the least significant of the most significant bits set should have more weight in terms of frequency increase/decrease than all of the least significant bits

combined. It can be seen from Figure 6-24 compared to Figure 6-23that there is finer control.

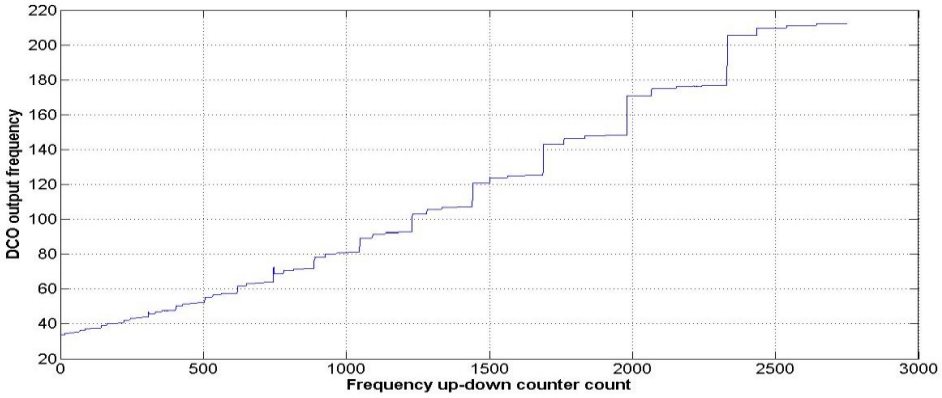


Figure 6-24 frequency vs. frequency up-down counter count – case iii

iv. A nonlinearity can be introduced to gain a finer frequency response and a wider range. Capacitors and current sources can have different weights. This situation is shown in Figure 6-25. A frequency range between 20 MHz and 212 MHz was obtained. The ratio between the highest frequency and the lowest frequency is more than 10. Since a non-monotonic response is present here, there are a set of forbidden numbers which the digitally controlled oscillator cannot see. Otherwise the system might get "stuck". This means the wide range and finer response comes at the cost of extra complexity.

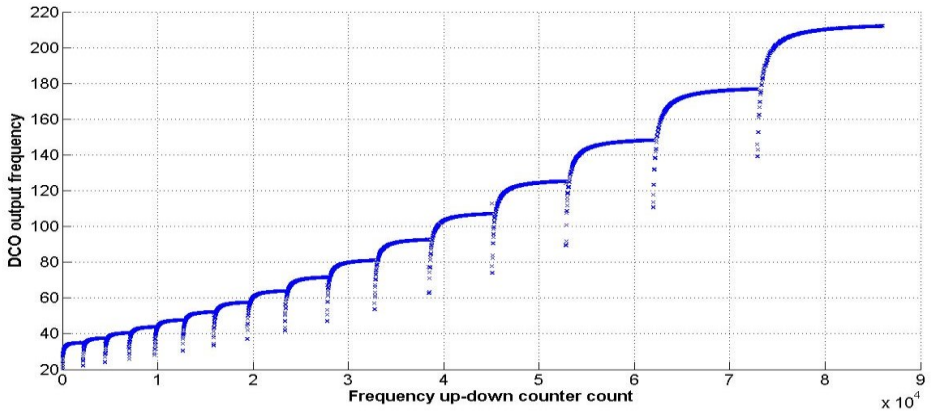


Figure 6-25 frequency vs. frequency up-down counter count – case iv

6.9 System level simulations

The system shown in Figure 6-2 was simulated for the case of an input coming at 100 MHz and the output shown in Figure 6-26 proves that digitally controlled oscillator locks at the frequency of the incoming signal after approximately 3.25μs. This time changes depending on the initial conditions of the digitally controlled oscillator. Because of the digital nature of the circuit, the digitally controlled oscillator output wiggles around 100MHz. This means that some of the bits in the frequency up – down counter flips between two values in order to generate the correct frequency. To gain more insight, it is useful to look at the DFT of the in-phase clock signal, I, shown in Figure 6-27. It is clear that the fundamental component is at 100MHz, even though, the frequency changes over time. It is also possible to see the third and the fifth harmonics.

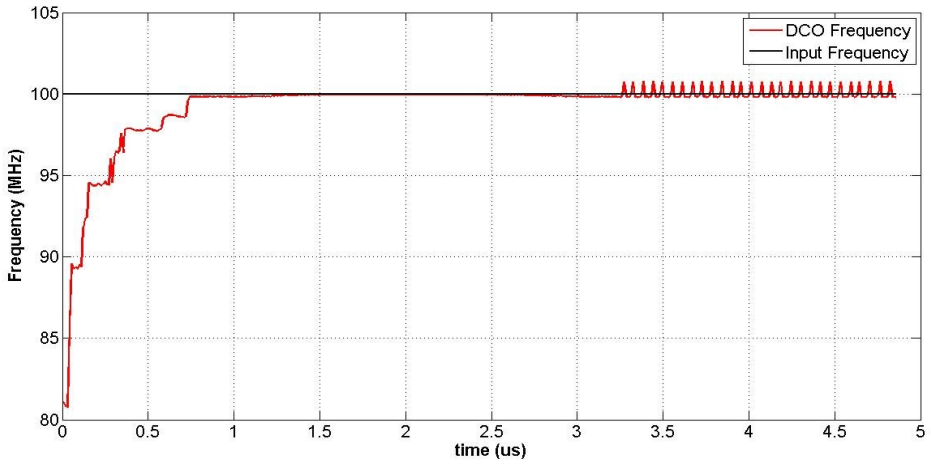


Figure 6-26 frequency vs. time for the incoming signal and the DCO (100MHz)

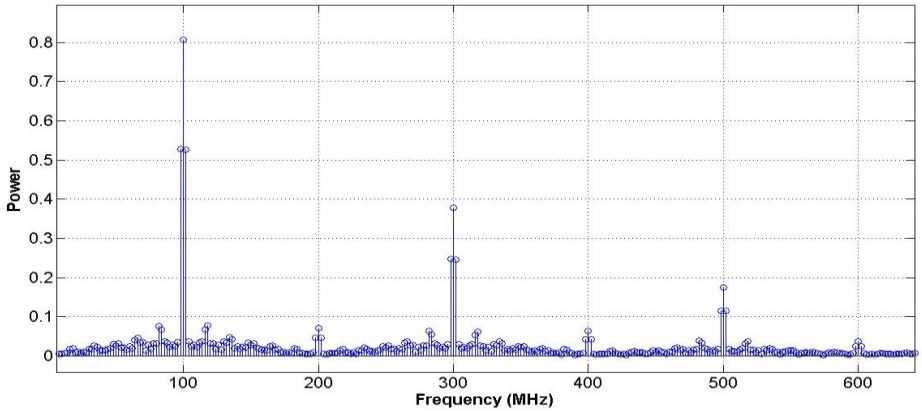


Figure 6-27 DFT of the DCO signal in lock (100MHz)

Another case is shown in Figure 6-28 where the initial frequency of the digitally controlled oscillator is at a higher frequency than the one of the incoming clock. Again, it is possible to see that the digitally controlled oscillator frequency is wiggling around 80MHz. Also, it can be seen that the oscillator takes around 6μs to lock. Figure 6-29 shows the DFT of the output signal in which it is possible to see that the fundamental component is precisely at 80MHz.

Finally, Figure 6-30 shows the in-phase clock, I, the quadrature phase clock, and the incoming clock in lock situation. It is clear that the in-phase clock, I, is in perfect synchronization with incoming clock while the quadrature phase is 90 degrees out of phase.

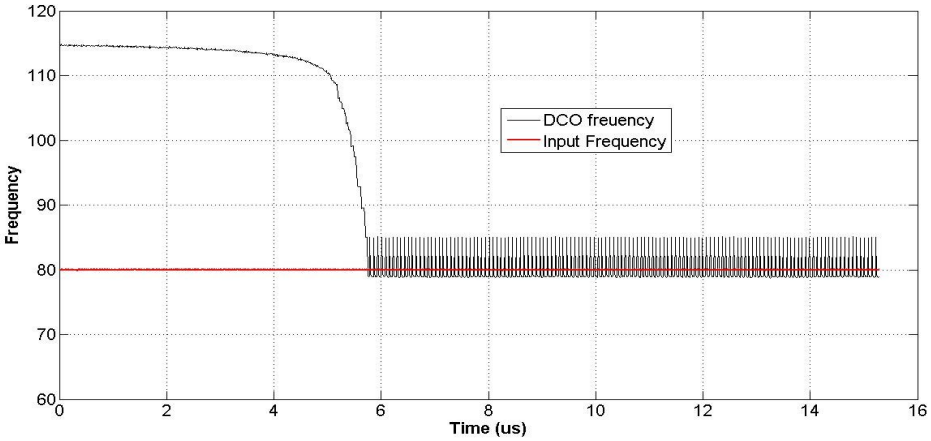


Figure 6-28 frequency vs. time for the incoming signal and the DCO (80MHz)

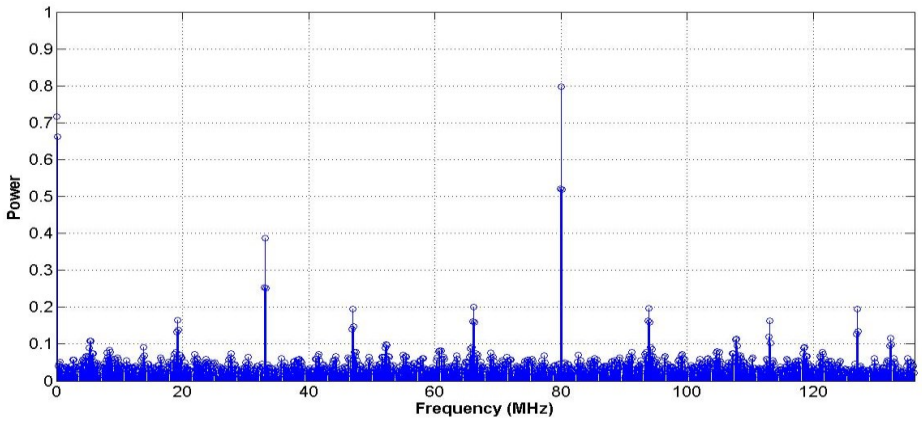


Figure 6-29 DFT of the DCO signal in lock (80MHz)

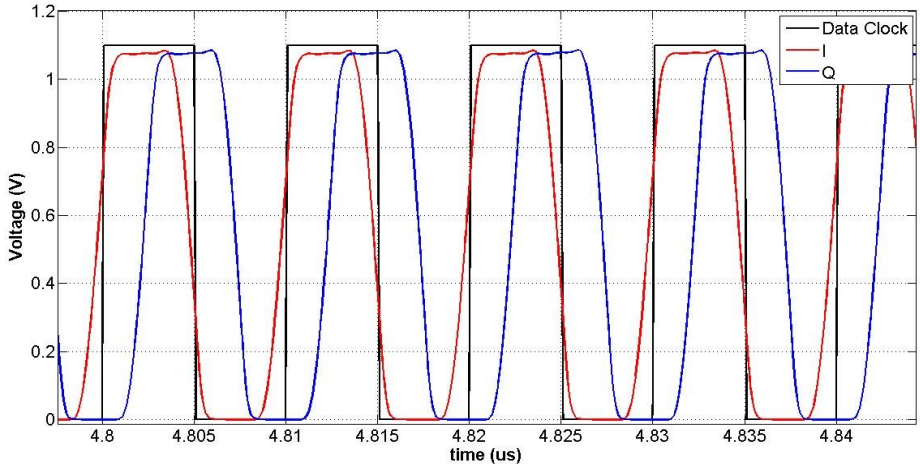


Figure 6-30 I, Q, and Incoming clock in-lock

6.10 Power consumption

In steady state, the primary source of power consumption is the oscillator. This is because the phase and the frequency detector consume very little power when in lock. Power consumption is highly dependent on the frequency, and the control technique used, i.e. if capacitors are present or if only current sources are present. To give an insight on the power consumption of this circuit, the current waveforms drawn from the supply at a frequency of 115MHz when only current sources control scheme is used is shown in Figure 6-31. The power consumption of this circuit is around 74μW. This makes it very suitable for ultra-low power receivers.

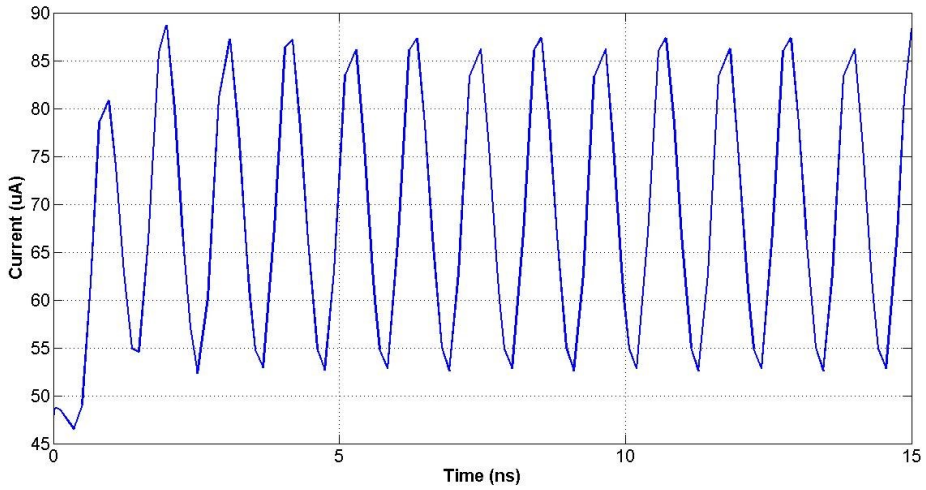


Figure 6-31 Oscillator current waveform

6.11 Other uses of this circuit

While the frequency detector only works with clock data input, the phase detector can also work and synchronize with random data. This means if a preamble is present to help the frequency detector lock on the correct frequency and then is turned off and since the phase detector can operate correctly with random data, and then this circuit

can function as a clock and data recovery circuit. The natural application of the clock and data recovery circuit is in optical communication system.

Moreover, since the number stored in the up-down counter corresponds to a particular frequency, this circuit also functions as an M-ary all-digital frequency demodulator. Assuming that the locking time is around 10μs and there are eight control bits. Then the data rate can be as fast as:

$$\frac{7}{10\mu s} = 7Mbit/s$$

Since in-lock the bits in the up-down counter wiggles between two values, two numbers can represent one frequency. For this reason, the number seven was used instead of eight.

Another advantage of this circuit is that it can operate with a broad range of data rates, many encoding techniques, and different standards. It is well suited to digital systems requiring an all-digital phase-locked loop or digital clock and data recovery circuit.

6.12 Compared to other designs

Compared to the state of the art, this implementation achieves very fast locking time due to its digital nature. Moreover, in nominal conditions, it can operate in the range 20 – 220 MHz while maintaining power consumption in the μW range. A brief comparison with some designs found in the literature is shown in Table 6-2. While it may seem that the range in narrow compared with other design, the ratio between the lowest and highest frequency is more than 10. Capable of operating at a data rate as low as 10MHz and as fast as 220MHz, this circuit is very useful in lower power all digital systems.

Table 6-2 PLL comparison with state of the art

Data rate range (Gbps)	Acquisition time	Paper
0.5 - 2.5	0.25ms	[41]
0.15 / 0.6 / 0.12 /2.5	25ms	[42]
0.0125 – 2.7	1ms	[43]
0.002 – 0.22	10μs <	This work

CHAPTER 7

Conclusions and future work

7.1 Conclusion

In this thesis, the design of a low power mm-wave transmitter with on-chip resonator and the design of a low power digital phase locked loop were discussed. Also, system level analysis was carried out.

The transmitter exhibit low power consumption while delivering adequate power to the antenna. This was achieved through a combination of ideas that included a high-Q on-chip resonator, an amplitude redistribution technique, and an enhancement of the differential Colpitts oscillator. Although the target application requires low data rate, the architectures discussed in this thesis promise high data rate – in the Mbit/s range. The transmitter architecture uses an on-chip resonator based on what was proposed in [17]. Using an on-chip resonator results in a small size transmitter requiring no external components while maintaining low power consumption.

A novel implementation of an all-digital phase-locked loop was proposed, and a transistor level implementation was simulated at the schematic level. Compared to the state of the art, this implementation achieves very fast locking time due to its digital nature. Moreover, in nominal conditions, it can operate in the range 20 – 220 MHz while maintaining power consumption in the μW range.

Four control techniques were studied and can be used to control the frequency of the ring oscillator. Each technique offers certain advantages at certain range of

operation frequencies. Three of the techniques studied require no change in the PLL except for the connection between the up-down counter of the frequency loop and the ring oscillator. The fourth technique, on the other hand, requires additional logic to be added. In terms of phase detection, Alexander phase detector has been shown to be a convenient choice for this type of digital phase locked loop and was employed in the design.

In terms of system-level analysis, the model developed succeeds in predicting the frequency of optimal power efficiency operation. It also suggests that higher frequencies are favorable in systems with constrained form factor. Optimal energy efficiency is achieved at the frequency at which the largest antenna in the form factor achieves impedance match.

7.2 Future work

The transmitter developed here is only one component of a larger system consisting of both a transmitter and a receiver. As a future work, the transmitter can be integrated with a receiver and with an on-chip antenna to form a complete transceiver. Within the transmitter, other types of on-chip resonators, such as a series resonance resonator can be tested and implemented within different transmitter architecture.

Regarding the digital phase locked loop, the fourth frequency control proposed in this thesis can be implemented which additionally requires the design of the additional logic block needed for proper interaction between the frequency detector and the ring oscillator. Further investigation of techniques to improve the operation frequency range could also be done.

In order to have a complete integrated circuit for the transmitter and the phase locked loop, the following tasks will have to be completed:

- Testing the two versions of the transmitter chip.
- Layout the phase locked loop, perform post-layout simulations, and tape-out.
- Experimental setup design and obtaining the experimental result in the lab to verify functionality and specifications.

The system level analysis can be improved by including a more realistic propagation model and include a more realistic transmitter model. The measurements can also be improved by redesigning the antenna in a way that eliminates the effect of the connector on antenna propagation.

Appendix A

LNA Design

A.1 Introduction

The LNA can be used to increase the sensitivity of the receiver or equivalently increase the maximum distance between the transmitter and the receiver. However, this comes at the cost of increased system power consumption. In this chapter, the design of a single stage LNA, shown in Figure A-1, will be explained.

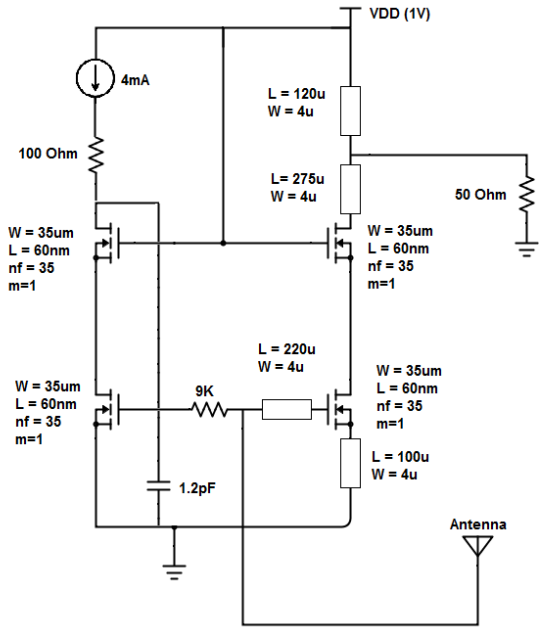


Figure A-1 LNA

A.2 Input and output matching

To achieve input matching, inductive source degeneration can be employed. By choosing the value of the inductor, it is possible to control the real part of the impedance seen when looking into the gate of the transistor. An inductively degenerated common-source amplifier is shown in Figure A-2:

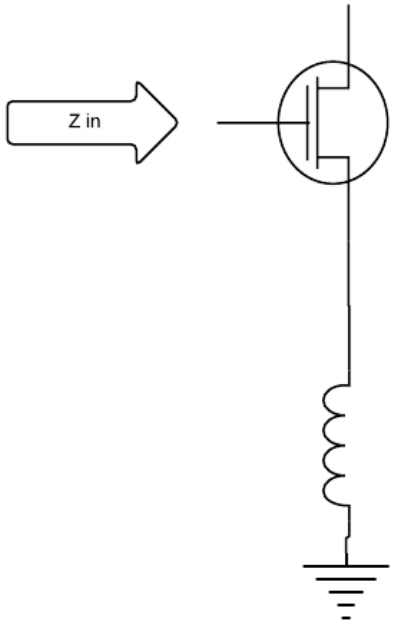


Figure A-2 inductively degenerated common source amplifier

From this circuit, the following small signal model can be obtained:

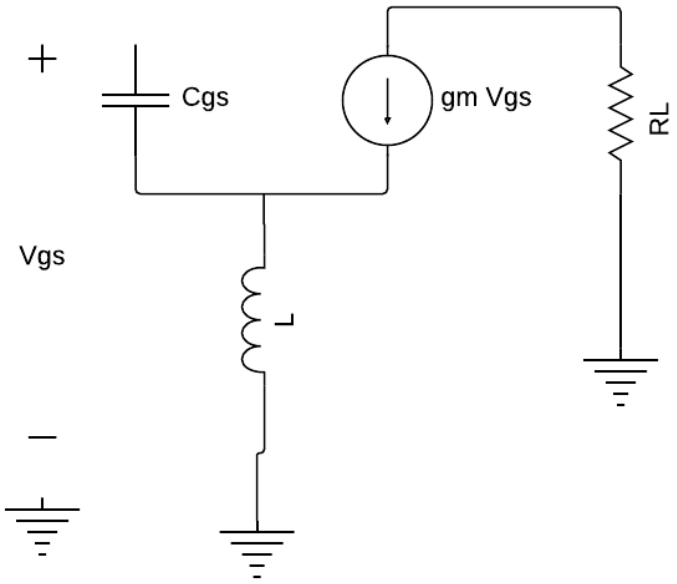


Figure A-3 Small signal model of an inductively degenerated common source amplifier

The following equation can be derived from the small-signal model for the input impedance of the amplifier:

$$Zin = sL + \frac{1}{sCgs} + \frac{gm}{Cgs} L \tag{A.1}$$

It is clear from the equation that the input impedance contains a resistive term proportional to the degeneration inductance value. Setting the resistive term to the impedance of the antenna, 50Ω, that is,

$$\frac{gm}{Cgs} L = 50\Omega \tag{A.2}$$

Implies that the resonance frequency is also set, that is

$$f_o = \frac{1}{2\pi\sqrt{L\,Cgs}} \tag{A.3}$$

Hence, another degree of freedom is needed to also set the resonance frequency. To achieve this, another inductor is connected to the gate of the transistor as shown in Figure A-4.

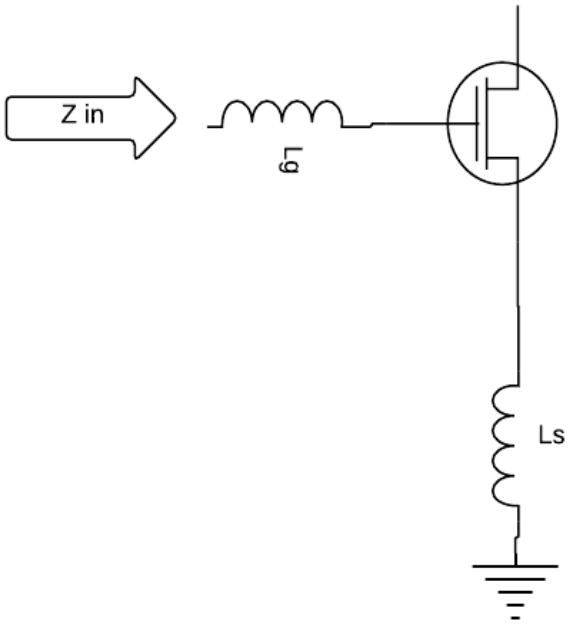


Figure A-4 inductively degenerated CS amplifier with an inductor in series with gate node

The input impedance, in this case, takes the following form:

$$Zin = s(Ls + Lg) + \frac{1}{sCgs} + \frac{gm}{Cgs}\, Ls \tag{A.4}$$

This way, it is possible to achieve input matching and setting the resonance frequency at the same time. The resonance frequency is given by:

$$f_o = \frac{1}{2\pi\sqrt{(Ls + Lg)\, Cgs}} \tag{A.5}$$

Inductors were realized using transmission lines to achieve input matching and the correct frequency.

Output matching is achieved through short circuited stub matching mainly because it is more convenient to use than lumped elements. The matching circuit is highlighted in:

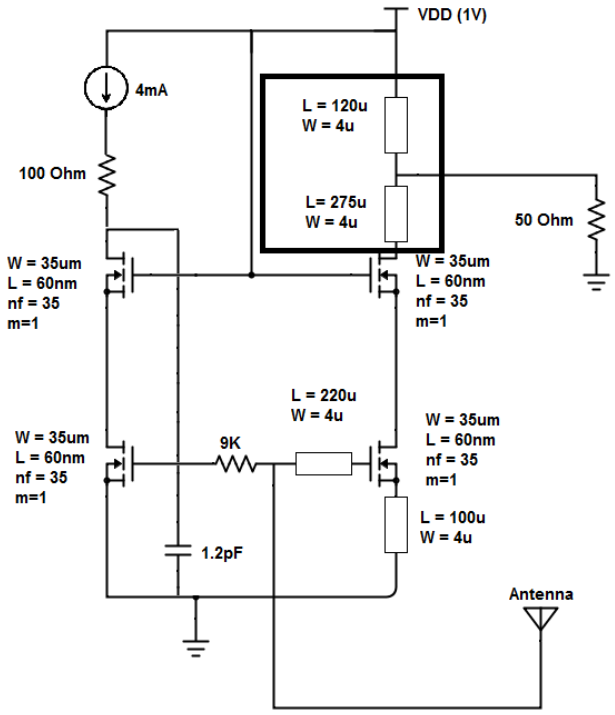


Figure A-5 Output matching circuit of the LNA

A.3 Biasing and noise optimization

As seen in Figure A-1, biasing is achieved through a simple current mirror. In order to reduce noise coming from the supply, a simple filter is used as shown.

According to [44], the absolute minimum noise figure is given by:

$$F_{min} \approx 1 + 2.3 \left[\frac{f}{f_t}\right] \tag{A.6}$$

where f_t is the cutoff frequency of this transistor. This means that the LNA should be biased at a current density corresponding to the highest cutoff frequency of the transistor. An indirect way to find this current density is by sweeping the biasing current and looking at the noise figure of the circuit. When the minimum value is achieved, then the biasing current at that point divided by the width of the transistor is required current density. Moreover, the number of fingers was optimized to achieve highest cutoff frequency.

A.4 Stability

Stern stability factor, K, was used to study the stability of this circuit. Stern stability factor is given by:

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}||S_{12}|} \quad \text{(A.7)}$$

where $\Delta = S_{11}S_{22} - S_{21}S_{11}$. In the case where $K > 1$ and $\Delta < 1$, the circuit is unconditionally stable.

A.5 Simulation results

s-parameters of this LNA are shown in Figure A-6. It is clear that the input and the output are both matched well at 60GHz. Moreover, a small signal gain of 8dB is achieved at 60GHz.

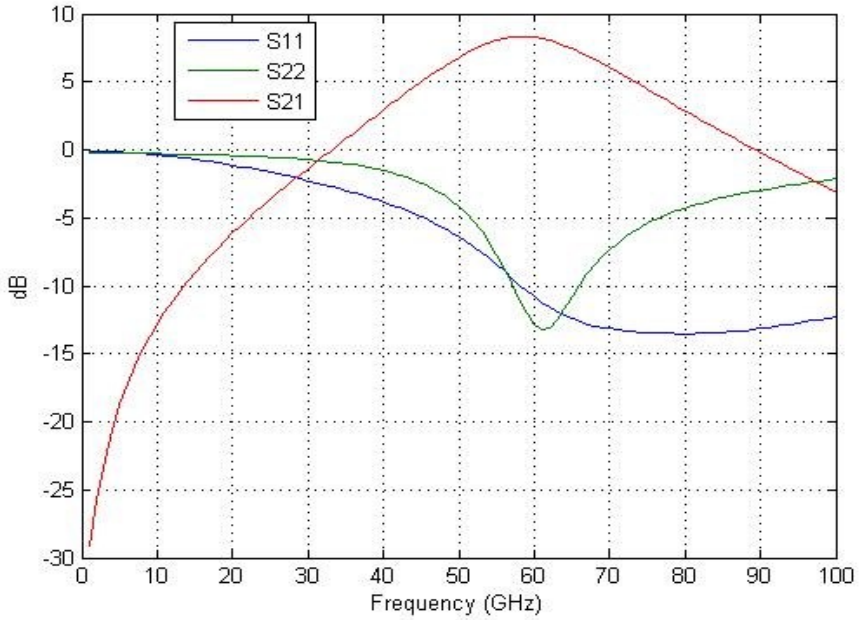


Figure A-6 LNA summary of simulation results

From stern stability factor, the circuit is unconditionally stable. The power consumption of this circuit is 8mW. The current density achieving highest cutoff

frequency is 0.22 mA/μm. Schematic level simulations show that a noise figure of 3.2dB is achieved. A summary of the specification achieved is given in Table A-**8-1**.

Table A-8-1 LNA specifications

Gain	8dB
Noise Figure	3.2dB
Power consumption	8mW
Supply voltage	1.1V
Stability	Unconditionally stable

A.6 Conclusions

The LNA as a whole was abandoned due to its high power consumption, 8mW, which was considered too high compared to the power consumption of the receiver. Thus, the receiver will interface directly with antenna through a matching network.

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