A Technology-Based Comparative Study for the Optoelectronic Integration of Optical Front-Ends

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***Abstract*—Optical receiver front-ends of varying technologies and packaging techniques are designed and compared. A 25 Gb/s monolithically integrated CMOS receiver consumes six times less power and three times less footprint than a discrete receiver.**

Keywords—optical receiver; electro-photonic integration.

An ever growing demand for higher package density and more energy efficient interface between photonic and electronic components of optical communication gear, e.g., in optical interconnects, calls for new technological solutions. One of the most promising approaches is the monolithic electro-photonic integration (EPI) of photonic devices, such as a photodetector, with analog electronics that provides an interface to ASIC, such as a transimpedance amplifier (TIA). EPI of this kind can be implemented in different technology platforms, each having its advantages and drawbacks. In this study, we investigate two such platforms, CMOS and heterojunction bipolar transistor (HBT) in indium phosphide (InP), from the viewpoint of their power efficiency and interface density. The subject of this current study is the receiver (RX) front-end, which comprises a photodetector and a TIA monolithically integrated onto one substrate. Through identification of metrics such as speed, power consumption, input sensitivity, and footprint area, the study extracts the current values of each platform for 10, 25, and 56 Gb/s applications. Advantages of the photonic/electronic co-design and monolithic integration are discussed by comparison with a conventional, discrete assembly approach. In discrete assembly, the photodetector and electronics may be designed by different entities and assembled through wire-bonding or flip-chip techniques.

A 25 Gb/s photodetector chip in GaInAs-InP (Do231_20um_C3 part from Global Communications Semiconductors, LLP) is experimentally characterized in terms of responsivity and small/large-signal response. From S-parameter and capacitance-voltage (CV) measurements, its junction capacitance, pad capacitance, and series resistance are obtained. Packaging the detectors with a commercial RX in a discrete fashion, via wirebonding, reveals an expected inductance range of 300 to 1000 pH.

In order to highlight the key differences between EPI and discrete assembly, only the transimpedance stage of the RX is designed. The design summarized in this report is based on the bulk CMOS TSMC 65nm technology node. For the discrete case, design is driven by the test-bench shown in Figure 1, which includes experimentally-verified *RLC* values. Simulations were conducted while the TIA was loaded with post-amplification stages that presented a load of approximately 30 fF. This is represented by C_{Load} for simplicity. Designs were catered to 25 Gb/s applications with a gain of 47 dBΩ to minimize the effect of noise from later stages.

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Once the TIA was designed in CMOS for discrete assembly with the photo-detector, as shown in Figure 1, it was re-designed for EPI, as shown in Figure 2. In EPI, the pad capacitances C_{pad_PD} and C_{pad_RX} no longer exist. Also, the junction capacitance value is modified to one that is representative of a silicon-based detector prepared from a bulk CMOS process [1]. The design for EPI reveals significant reduction in power consumption as well as in device footprint area, as summarized in Table I.

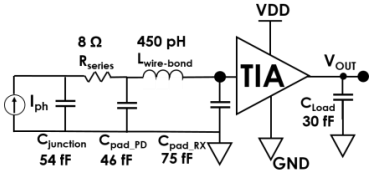

Fig. 1. TIA design test-bench for discrete assembly with photo-detector.

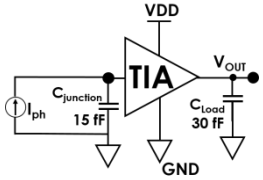

TABLE I – IMPROVEMENT FOLD FOR MONOLITHIC INTEGRATION

Parameter	Value
Device area reduction	3
Power reduction	6
Noise increase	1.2

Fig. 2. TIA design test-bench for electro-photonic integration (EPI).

As data rate and gain were matched for both scenarios in Table I, the input referred RMS noise current increase for EPI is partially affected by the physical *kT/C*-noise dependence. Nonetheless, CMOS-compatible photodetectors such as Ge-based detectors benefit from greater responsivity with increased junction capacitance. This allows for an optimized co-design of the photonics and electronics to regain the input sensitivity through these two mechanisms: 1) improved responsivity of the detector, and 2) lower *kT/C* noise. An ability to co-design the photodetector and TIA to the best of the resulting integrated RX front-end performance is, along with the mitigation of wire-bonding need, a non-trivial advantage of EPI. From this point of view, both CMOS and HBT in InP based platforms are capable and promising for higher data rate demand. Which one to choose strongly depends on the application, with CMOS-based platforms being less power hungry while HBT in InP-based platform being more cost efficient at higher data rates.

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