Integrated RF Passive Low Pass Filters in Silicon Photonics

Mohammadreza Sanadgol Nezami, Bahaa Radi, Amit Gour, Yule Xiong, Mohammad Taherzadeh-Sani, Michaël Ménard, *Member IEEE*, Frederic Nabki, *Member IEEE*, and Odile Liboiron-Ladouceur *Senior IEEE Member*

***Abstract*— The integration of passive radio frequency (RF) components, such as resistors, capacitors, and inductors, requires a relatively large area on complementary metal oxide semiconductor (CMOS) chips, which is not cost-effective in developing optical receiver front-ends. This could be addressed by implementing passive RF components on silicon photonics chips. In this work, we present an on-chip passive RF low-pass filter coupled to an integrated photodetector. This study demonstrates that passive RF analog processing can be implemented in a commercial silicon photonics platform. The performance of the implemented RC filters is reported at frequencies up to 15 GHz.**

***Index Terms*— passive RF circuits, low pass filters, photonic integrated circuits, CMOS integrated circuits, silicon photonics**

I. Introduction

Passive radio frequency (RF) elements such as inductors, capacitors, and resistors are necessary in high-speed optical transceivers. However, the bulky nature of passive RF components prevents further miniaturization of the RF chips for cost-effective high-speed applications. This limitation can be partially overcome by using off-chip components at the cost of a reduced level of integration and additional parasitics from the package. With the increased importance of RF passive elements in applications such as oscillators [1], passive equalizers [2], and data serializers / deserializers [3], it is worth considering alternative integration schemes with other optical/electrical components.

Authors acknowledge the support from Canadian Microelectronic Corporation (CMC) for the subsidized MPW fabrication through A*STAR Institute of Microelectronics, and the financial support from the Natural Sciences and Engineering Research Council of Canada (NSERC) Idea to Innovation (I2I) program. The authors would like to thank Dan Deptuck and Alireza Samani for their help.

M. S. Nezami, B. Radi, Y. Xiong, and O. Liboiron-Ladouceur are with the Department of Electrical and Computer Engineering, McGill University, Montreal, QC, H3A 0G4, Canada. (email: mohammadreza.sanadgolnezami@mcgill.ca, bahaa.radi@mail.mcgill.ca, yule.xiong@mail.mcgill.ca, odile.liboiron-ladouceur@mcgill.ca).

Mohammad Taherzadeh-Sani is with the Department of Electrical Engineering, Ferdowsi University of Mashhad, Mashhad, Iran. (Email: taherzadeh@um.ac.ir)

M. Menard is with the Department of Computer Science, Université du Québec à Montréal, Montréal, H2L 2C4, Canada. (email: menard.michael@uqam.ca)

F. Nabki and A. Gour are with the Department of Electrical Engineering, École de Technologie Supérieure, Montréal, H3C 1K3, Canada. (email: frederic.nabki@etsmtl.ca, amit.gour.1@ens.etsmtl.ca)

The monolithic integration of electronic and photonic components on silicon is the most advantageous solution to minimize parasitics between the optical and electronic circuits. Electronic circuits have been implemented in silicon photonic fabrication processes [4, 5] but the transistors used have been limited to the 130 nm and 90 nm nodes. Another approach to achieve monolithic integration with higher performance electronic nodes has been to build optical devices with almost no modification to the electronic fabrication process [6]. However, the trade-off in this case is a reduction in the performance of the optical devices. Therefore, hybrid integration enables the use of state-of-the-art photonic integrated circuits (PICs) and complementary metal oxide semiconductor (CMOS) integrated circuits (ICs) in the same system [7]. Furthermore, the parasitics at the interface between the chips can be minimized with advanced system-in-a-package technologies, such as flip-chip bonding [8].

Silicon photonics provides a potentially cost-effective platform for the integration of photonic components with RF passive elements. This offers great opportunities to develop high-speed transceiver modules by co-packaging the PIC and the CMOS IC [9]. Furthermore, as processing speeds increase, one issue is the increased cost of integrating passive RF components on the CMOS chip as their size relative to the transistor circuit becomes significantly larger. This increase in cost of fabrication is especially noticeable for smaller CMOS technology nodes. For example, the cost per mm^2 of STMicroelectronics 28 nm fully depleted silicon-on-insulator CMOS process is at least 17 times more expensive than that of Advanced Micro Foundry (AMF) Silicon Photonics technology (prices provided by CMC Microsystems) [10]. Moreover, since the typical minimum feature size in silicon photonics is above 100 nm, the fabrication can be done with less advanced photolithography tools than high-speed CMOS circuits. In addition to the cost advantage, silicon photonics benefits from a high-resistivity substrate. It has been shown that high-resistivity substrates facilitate the suppression of substrate noise and crosstalk and increase the quality factor (Q) of RF passive components [11-14].

In this work, we investigate the potential of silicon photonics to implement RF electrical passives integrated elements by demonstrating three variations of an RC low pass filter (LPF) monolithically integrated with a photodiode (PD). This proof-of-concept validates the potential for cost-effective receiver

front-end designs. The model, the design strategy and fabrication process are presented in the subsequent sections. The scattering parameters (S-parameters) of the electrical signal at the output of the photodiodes are measured and analyzed. Finally, an equivalent circuit is used to validate the behavior of the fabricated devices for parameter extraction.

II. Circuit Model and Design Parameters

Figure 1 presents a schematic diagram of a lumped model for the PD and the LPF. The PD, the filter resistor, and the filter capacitor are connected in a parallel configuration. In the circuit model, the LPF has a designed resistance R_f, and a designed capacitance C_f. The current source I_{PD} models the photocurrent. At a reverse bias voltage of 2 V, the PD has a junction capacitance C_j and a series resistance R_s which are around 35.2 fF and 85 Ω, respectively [15]. The metallic pads of the PIC add parasitics represented by the capacitance C_{pad}, which is about 15.2 fF for a pad size of 70×70 μm^2 [15]. From our simulations, the estimated value of the pad resistance R_{pad} is 4 Ω, and the inductance L_{pad} is 0.17 nH. The load resistor R_L models the 50 Ω measurement equipment termination resistance.

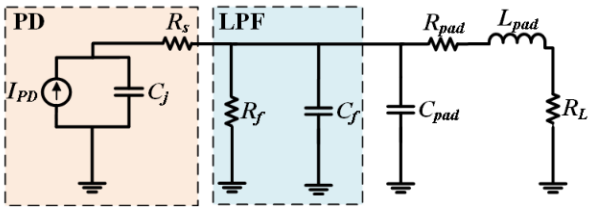

Fig. 1: Schematic of the circuit model for the designed RC low pass filters. Dashed boxes outline the PD and LPF configurations.

The 3-dB bandwidth (f_{3dB}) of the receiver front-end is determined by the poles estimated using the open circuit time constant approach. This method is an approximate analysis for the estimation of the cut-off frequency of the electronic circuit. It estimates the cut-off frequency by summing the RC time constant of all the capacitors in the circuit [16]:

$$C' = C_f + C_{pad}\,, \tag{1}$$

$$f_{3dB} = \frac{1}{2\pi(\tau_1+\tau_2)} \approx \frac{1}{2\pi\tau_1}, \tag{2}$$

$$\tau_1 = C'\big(R_f \parallel (R_L + R_{pad})\big), \tag{3}$$

$$\tau_2 = C_j\big(R_s + R_f \parallel (R_L + R_{pad})\big), \tag{4}$$

where τ_1 and τ_2 are the time constants associated with C' and C_j, respectively, such that $C' \gg C_j \Rightarrow \tau_1 + \tau_2 \approx \tau_1$. As can be seen, the LPF parameters, C_f and R_f, are dominant parameters in determining the 3-dB bandwidth of the filter.

The designed silicon photonics receiver front-end is fabricated on a SOI wafer with a 220 nm silicon device layer and a 2 μm buried oxide layer, and a silicon substrate of 725 μm with a resistivity greater than 750 Ω.cm. The SiGe vertical PDs have a thickness, width, and length of 0.5 μm, 8 μm, and 31 μm, respectively. The PDs consist of a highly doped n-type germanium layer, an intrinsic germanium layer, and a p-type silicon layer [17]. The dimensions of the plates for the metal-dielectric-metal (MIM) capacitors were estimated by using the design strategy detailed in [18]. The capacitors consist of two aluminum layers, corresponding to Metal 1 and Metal 2 in the fabrication process, that are 0.75 μm and 2 μm thick, respectively. A 1.5 μm thick SiO_2 layer is sandwiched between the metal layers to form the capacitor dielectric. Figure 2(a) shows the cross-section view of the MIM capacitor. The resistors are formed on a 0.09 μm thick n-type silicon layer with a doping density of at least 10^{20} cm^{-3} [19]. Figure 2(b) shows a micrograph of one of the implemented LPF structures integrated with a p-i-n PD.

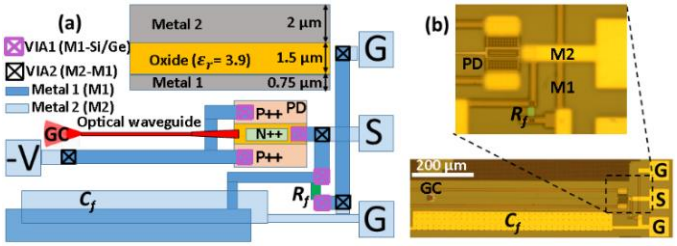

Fig. 2: (a) Cross-section view of the MIM capacitor and layout view of the LPF structure (GC: grating coupler, PD: photodiode, M1: Metal 1, M2: Metal 2) (b) Micrograph of the RC filter structure in an active silicon photonics process.

To achieve cut-off frequencies ranging from 1.5 to 2.7 GHz, the target values for the resistors are 160 Ω and 400 Ω, and for the capacitors, they are 1.35 pF and 2.34 pF. The estimated length and width of the metal plates for a 1 pF capacitor are 708 μm and 67 μm and for a 2 pF capacitor they are 708 μm and 33.5 μm. It has been shown that the fringing electric fields on the perimeter of the integrated capacitors lead to additional capacitance in the microstructures [20]. The fringing field capacitance can be estimated using the ANSYS HFSS 3D electromagnetic field simulator. Based on the HFSS simulation results, the expected capacitance values including the effect of the fringing field capacitance for the 1 pF and 2 pF MIM capacitors are of 1.35 pF and 2.34 pF, respectively.

The LPF resistor values were designed using the mathematical relationship $= \rho\, l/A$, where ρ is the resistivity of the doped region, l is the length of the resistor, and A is the cross-section area of the resistor. Assuming a linear behavior of the integrated resistor at 300 K, a doping density of 10^{20} cm^{-3}, and a resistivity of 7.2×10^{-4} Ω.cm [21], a 160 Ω resistance is obtained by choosing a length of 10 μm and a width of 5 μm for the doped region. Similarly, a length of 25 μm with the same width leads to a 400 Ω resistance.

Using the lumped model shown in Fig. 1, simulations with the Advanced Design System (ADS) software from Keysight were performed to fits the S-parameter curves obtained through the experimental measurements. Table I summarizes the parameters of the circuit model. As the junction capacitance C_j is much smaller than the filter capacitance C_f, the parameters of the filter defines the location of the dominant pole. The PD and pad parameters have negligible effects on the overall performance of the filter. LPF1, LPF2, and LPF3

are associated with the designed values of R_1=400 Ω and C_1=1.35 pF, R_2=160 Ω and C_2=2.34 pF, and R_3=400 Ω and C_3=2.34 pF, respectively. Using equations (1) to (4), the expected 3-dB cut-off frequencies are 2.65 GHz, 1.78 GHz, and 1.53 GHz, respectively.

TABLE I
EQUIVALENT CIRCUIT PARAMETERS

Parameter	Value
R_s	85 Ω[1]
C_j	35.2 fF[1]
C_{pad}	15.2 fF[1]
R_{pad}	4 Ω[2]
L_{pad}	0.17 nH[2]
R_L	50 Ω

[1] Values reported in [15]
[2] Values extracted from simulations.

III. Experimental Results

Three chips were tested, and were numbered 1, 2 and 3 for reference. The implemented resistances were directly measured on the chip using an RF Ground-Signal-Ground (GSG) probe and an ohmmeter. Because of the presence of the PD junction capacitance and other stray capacitors in the structure, direct measurement of the capacitance on the chip does not give an accurate value of the filter capacitance at a specific frequency. Thus, the impedance fitting technique with a lumped model was used in the ADS software to extract the capacitance. Measurements of the S-parameters were performed with a 50 GHz lightwave component analyzer (Agilent N4373C) with a 2-V reversed bias applied to the PDs. The effects of the RF cables and probe tip were removed from the measurements by following a procedure relying on a calibration kit and a calibration substrate.

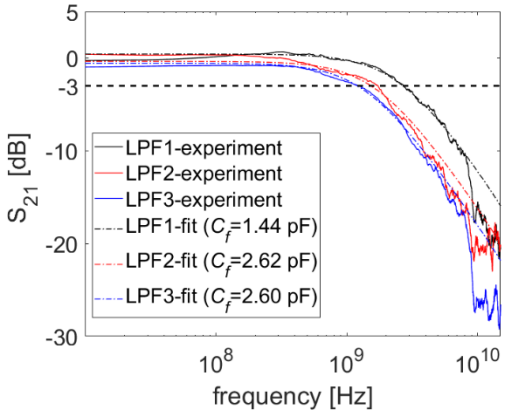

Fig. 3: Measured and fitted S_{21} parameter using the lumped model shown in Fig.1 and the parameters values in Table I for chip no. 3 at 2 V reverse bias.

The lightwave component analyzer was used to perform optical-electrical measurements by generating modulated light that is coupled to the chip. The optical signal travels through the waveguide on the PIC to the PD. Then, the PD converts the optical signal into an electrical one that the analyzer measures and from which it extracts the S21 value that characterizes the optical-electrical conversion. To match the simulation and experimental results of the S_{21} parameters, the optimization performs a parameter sweep for the low-pass filter capacitance C_f. To this end, a goal is defined based on the measured cut-off frequencies. Figure 3 shows the measured and simulated S_{21} parameters for chip no. 3, after optimization of the model. The simulated cut-off frequencies using the equivalent circuit with the optimized parameters match the experimental values. Figure 4 compares the measured and simulated S_{22} parameters (output return loss) for chip no. 3 in a Smith chart format giving a polar representation of the reflection coefficients. At any given frequency, both the magnitude and phase information from the experiment on the fabricated structures and their impedance-matched models can be derived from the chart. The results represented in Fig. 4 confirm the validity of the lumped model component values after performing the impedance fitting. The measured return loss is in good agreement with the return loss obtained from the lumped model (Fig. 1) over the whole frequency range. Assuming a characteristic impedance of $Z_0 = 50\,\Omega$, the measured normalized impedance (solid red plot), $^{Z}/_{Z_0}$, at the cut-off frequency of 1.56 GHz for LPF2 on chip no. 3 is 0.523-j1.063 and the normalized impedance derived from the model (dashed red plot) at the cut-off frequency of 1.67 GHz is 0.448-j0.928, which shows a good impedance correspondence between the lumped model and the implemented structure.

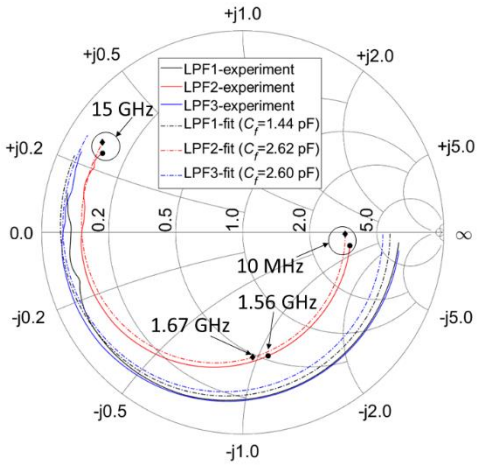

Fig.4: Measured and fitted S_{22} parameter using the lumped model shown in Fig.1 and the parameters values in Table I for chip no. 3 at 2 V reverse bias

Table II compares the experimental values of C_f and R_f with the target design values for three chips from the same wafer. The target design values are shown in the brackets.

TABLE II
MEASURED VERSUS DESIGNED CAPACITANCE (PF) AND RESISTANCE (Ω)

Chip	LPF1		LPF2		LPF3	
	R1 (400)	C1 (1.35)	R2 (160)	C2 (2.34)	R3 (400)	C3 (2.34)
1	416	1.49	168	2.55	412	2.31
2	427	1.45	171	2.45	421	2.61
3	407	1.44	165	2.62	406	2.60

From these results, it can be inferred that the experimental results are up to 12 % larger than the designed values. The uneven thickness of the oxide between the capacitor metal plates due to the fabrication process variations can be the main cause of difference. An oxide thickness variation of at least

10 % is expected on the fabricated chips. Furthermore, variation in the dimensions of the metal plates during the metallization process is another factor that plays a role in the observed difference in the capacitance values. The differences in the resistance between dies are attributed to variations in the resistor doped area dimensions after fabrication and in the doping density of the silicon. There are small discrepancies between the designed and measured resistance values that are due to the effect of the pad resistance and fabrication process variations. In particular, a lower doping density of the n-Si [22] and a smaller Si thickness [23] in the resistor areas can lead to a larger resistance. While insufficient data is available to perform an accurate statistical analysis to compare these results with their CMOS counterparts, the presented results for three chips show small chip-to-chip variations for the resistors and capacitors on the PICs. It should be noted that, chip-to-chip variation in the capacitor and resistor values in CMOS processes are significant [24]. For instance, simulation results in a 65 nm CMOS technology show a ±10 % and ±30 % chip-to-chip variation in the values of MIM capacitors and silicided poly resistors, respectively.

Table III summarizes the cut-off frequencies that resulted from the measurement and the lumped model in comparison with the designed values for the three different chips. There is a good agreement between the experimental results for the different dies. However, the measured cut-off frequencies for three instances of LPFs are slightly less than the expected cut-off frequencies from the designed values. These discrepancies are likely caused by an increase in the effective value of passive elements (e.g., capacitors) resulting from fabrication process variations and fringing fields as discussed earlier.

TABLE III
FILTER 3-DB CUT-OFF FREQUENCIES (GHZ)

Chip ID	LPF1		LPF2		LPF3	
	Design: 2.65		Design: 1.78		Design: 1.53	
	Fit	Meas.	Fit	Meas.	Fit	Meas.
1	2.65	2.67	1.69	1.61	1.38	1.41
2	2.69	2.72	1.70	1.65	1.22	1.24
3	2.71	2.75	1.67	1.56	1.21	1.23

IV. CONCLUSION

In this work, RC LPFs were implemented on a PIC as a case study to show that bulky passive RF components in a receiver front end can be built with silicon photonics. To investigate the performance of integrated RF components on the PIC, S-parameters for three RC filters were analyzed. A circuit model was used to evaluate the design strategy. The capacitor values of the filters were extracted using the ADS optimization tool. Considering the effect of fringing field capacitance, the extracted values from the experiment are in agreement with the expected values. Furthermore, chip-to-chip variations comparable to that of CMOS IC designs were observed. This validates the circuit model and demonstrates the feasibility of implementing passive components on PICs.

REFERENCES

[1] J. Geng, L. Zhang, C. Zhu, L. Dai, X. Shi, and H. Qian, "An Oscillator-Based CMOS Magnetosensitive Microarray Biochip With On-Chip Inductor Optimization Methodology," *IEEE Trans. Microw. Theory Tech.*, vol. 66, no. 99, pp. 1–14, May 2018.

[2] S. Tanaka *et al.*, "Ultralow-Power (1.59 mW/Gbps), 56-Gbps PAM4 Operation of Si Photonic Transmitter Integrating Segmented PIN Mach–Zehnder Modulator and 28-nm CMOS Driver," J. Lightwave Technol., vol. 36, no. 5, pp. 1275–1280, Mar. 2018.

[3] M. S. Hai, M. Ménard, and O. Liboiron-Ladouceur, "Integrated optical deserialiser time sampling based SiGe photoreceiver," *Opt. Express*, vol. 23, no. 25, p. 31736, Dec. 2015.

[4] C. Xiong, D. M. Gill, J. E. Proesel, J. S. Orcutt, W. Haensch, and W. M. J. Green, "Monolithic 56 Gb/s silicon photonic pulse-amplitude modulation transmitter," *Optica*, vol. 3, no. 10, pp. 1060–1065, Oct. 2016.

[5] A. Narasimha *et al*., "A Fully Integrated 4×10-Gb/s DWDM Optoelectronic Transceiver Implemented in a Standard 0.13µm CMOS SOI Technology," IEEE J. of Solid-State Circuits, vol. 42, no. 12, pp. 2736–2744, Dec. 2007.

[6] V. Stojanović *et al.*, "Monolithic silicon-photonic platforms in state-of-the-art CMOS SOI processes [Invited]," *Opt. Express*, vol. 26, no. 10, pp. 13106–13121, May 2018.

[7] T. Baehr-Jones *et al.* "Myths and rumours of silicon photonics," *Nat. Photonics*, vol. 6, no. 4, pp. 206-208, Mar. 2012.

[8] P. D. Dobbelaere *et al.*, "Advanced silicon photonics technology platform leveraging a semiconductor supply chain," in *IEDM*, San Francisco, CA, USA, 2017, pp. 34.1.1-34.1.4.

[9] A. E. Lim *et al*., "Review of Silicon Photonics Foundry Efforts," IEEE J. Sel. Topics in Quantum Electron., vol. 20, no. 4, pp. 405–416, Jul. 2014.

[10] Pricing, F. (2018). Fabrication and Pricing | CMC Microsystems. [online] Available at: https://www.cmc.ca/en/WhatWeOffer/Make/FabPricing.aspx [Accessed 18 Sep. 2018].

[11] J. P. Raskin, "SOI technology: An opportunity for RF designers?," in *VLSI-DAT*, Hsinchu, Taiwan, Jun. 2014, pp. 1–2.

[12] K. Benaissa *et al*., "RF CMOS on high-resistivity substrates for system-on-chip applications," *IEEE Trans. Electron Devices*, vol. 50, no. 3, pp. 567–576, Mar. 2003.

[13] J.- Raskin, A. Viviani, D. Flandre, and J.- Colinge, "Substrate crosstalk reduction using SOI technology," *IEEE Trans. Electron Devices*, vol. 44, no. 12, pp. 2252–2261, Dec. 1997..

[14] T. Zheng, M. Han, G. Xu, L. Luo, and T. Zheng, "Design and fabrication of suspended high Q MIM capacitors by wafer level packaging technology," in *ICEPT*, Changsha, China, 2015, pp. 89–94.

[15] M. M. P. Fard, G. Cowan, and O. Liboiron-Ladouceur, "Responsivity optimization of a high-speed germanium-on-silicon photodetector," Opt. Express, vol. 24, no. 24, pp. 27738–27752, Nov. 2016.

[16] A. S. Sedra and K. C. Smith, Microelectronic circuits. Oxford, NY, USA: Oxford University Press, 2004, pp. 575-578.

[17] J. M. Lee, S. H. Cho, and W. Y. Choi, "An Equivalent Circuit Model for a Ge Waveguide Photodetector on Si," *IEEE Photon. Technol. Lett.*, vol. 28, no. 21, pp. 2435–2438, Nov. 2016.

[18] M. S. Hai, M. N. Sakib, and O. Liboiron-Ladouceur, "A 16 GHz silicon-based monolithic balanced photodetector with on-chip capacitors for 25 Gbaud front-end receivers," *Opt. Express*, vol. 21, no. 26, pp. 32680–32689, Dec. 2013.

[19] L. Chrostowski and M. Hochberg, Silicon photonics design: from devices to systems. Cambridge University Press, 2015.

[20] W.-C. Chuang, C.-W. Wang, W.-C. Chu, P.-Z. Chang, and Y.-C. Hu, "The fringe capacitance formula of microstructures," J. Micromech. Microeng., vol. 22, no. 2, p. 025015, Jan. 2012.

[21] Irvin John C., "Resistivity of Bulk Silicon and of Diffused Layers in Silicon," *Bell System Tech. Journal*, vol. 41, no. 2, pp. 387–410, Mar. 1962.

[22] K. Takeuchi, A. Nishida, and T. Hiramoto, "Random Fluctuations in Scaled MOS Devices," in *SISPAD*, San Diego, CA, USA, Oct. 2009, pp. 1–7.

[23] W. A. Zortman, D. C. Trotter, and M. R. Watts, "Silicon photonics manufacturing," Opt. Express, vol. 18, no. 23, pp. 23598–23607, Nov. 2010.

[24] A. Aktas and M. Ismail, "CMOS PLL calibration techniques," IEEE Circuits Devices Mag., vol. 20, no. 5, pp. 6–11, Sep. 2004.