Comparative Study of Optoelectronics Receiver Front-End Implementation in InP, SiGe, and CMOS

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Abstract— **A comparison between typical optoelectronic receiver front-end implemented using CMOS, SiGe BiCMOS, and InP technologies in terms of sensitivity and power consumption is presented. We discuss important design trade-offs in these technologies including monolithic versus hybrid integration of the photodetector with the TIA on-chip.**

I. Introduction

As recent statistics indicate the number of internet nodes is expected to increase from 8.7 billion devices in 2012 to 50.1 billion devices in 2020 [1], there has been an explosive demand for high-speed optical communication systems. This demand is driving the need for high-speed and low power electronic front-ends with high sensitivity to the input optical power. Indium phosphide (InP) technology is conventionally used for the design of the electronic front-ends because of their high transition frequency, and for the possibility of monolithically integrating the photodetector on-chip with the transimpedance amplifier (TIA). This approach can be implemented in SiGe technology as well. With miniaturization, however, the transition frequency of CMOS technologies is becoming comparable to that of the InP technology. Fig. 1 shows the transition frequency of 32 nm, 45 nm, 65 nm, 90 nm CMOS technology, 130 nm SiGe, and 130 nm InP technologies [2]-[4]. From Fig. 1, it can be seen that the 32 nm CMOS node has a transition frequency of 450 GHz comparable to that of the InP technology of 520 GHz. Hence, CMOS continues to dominate areas once claimed by InP technology. The trend line for CMOS transition frequency is also shown in Fig. 1.

In this paper, we expand on our comparative study in [5]. Here, TIAs implemented in the three technologies are compared with respect to their input signal sensitivity and power consumption at 40 Gb/s and 50 Gb/s. In this comparison, we consider conventional TIAs and exclude other front-end design approaches. Receivers with equalizers are excluded due to their higher power consumption, and we also exclude receivers utilizing low bandwidth TIAs such as in [6]. To the authors' best knowledge, similar designs are not yet reported in InP nor in SiGe BiCMOS making the comparative analysis difficult.

II. Technology Trend Discussion

In a conventional optical receiver front-end, the input stage is the TIA providing a low input impedance path to the photocurrent generated by the photodetector. The TIA converts the photocurrent to a voltage through a transimpedance for further processing through the receiver chain. From a system point of view, sensitivity, power consumption, and data rate are the more important design specifications of the transimpedance amplifier. Other important design considerations include footprint which will be briefly discussed in this paper, supply voltage that is inherent to the technology and what the designer can do little about, and the transimpedance. The transimpedance of the designs compared in this section are sufficient to generate the voltage required for processing down the receiver chain. Hence, we focus our attention on sensitivity, data rate, and power consumption in the comparison. Reported state-of-the-art TIAs are compared in terms of their sensitivity and power consumption. Specifically, TIAs implemented in the three technologies of interest are investigated with data rates of 40 Gb/s and 50 Gb/s.

The sensitivity of a TIA circuit (i_{sens}) relates to the input referred noise ($i_{n,in}$) taking into account the bandwidth (BW) of the TIA and the signal-to-noise ratio (SNR) required to achieve a specific bit error rate (BER) through (1) [7].

$$i_{sens} = SNR \times \sqrt{\overline{i_{n,in}^{\,2}} \times BW} \qquad (1)$$

For a BER of 10^{-12}, the required SNR is 14 dB assuming Gaussian noise [8]. A photodetector responsivity of 0.7 A/W is assumed to obtain the optical power sensitivity. This conversion is necessary for designs that do not report

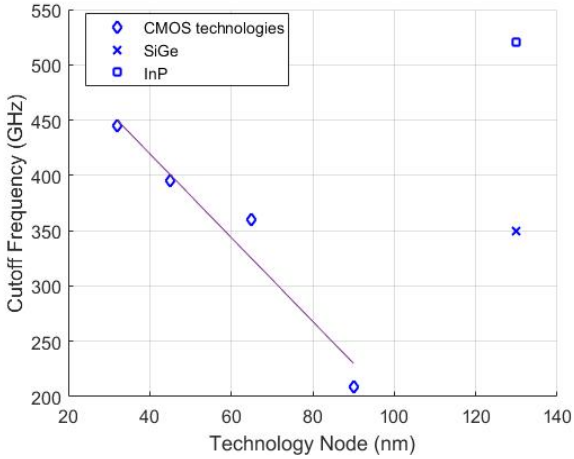

Fig. 1. Transition frequency of 32 nm, 45 nm, 65 nm, 90 nm CMOS (with shown trend line in purple), 130 nm SiGe, and 130 nm InP technologies.

optical sensitivity and only report input referred noise.

Fig. 2 and Fig. 3 show the optical power sensitivity and the power consumption of TIAs [9-27] suitable for operation at 40 Gb/s and 50 Gb/s, respectively. Fig. 2 shows that for designs achieving similar sensitivity at the same data rate, the power consumption of CMOS is lower than that of InP and SiGe. While [17] achieves a sensitivity of -14 dBm, approximately 6 dB better than other designs at 40 Gb/s, a few recent designs in CMOS [20-21] achieve similar sensitivity at 50 Gb/s (Fig. 3).

This state-of-the-art overview can lead one to conclude that TIAs implemented in CMOS are more energy-efficient. However, this comes at the cost of implementing a separate photodetector (PD) which adds parasitics in the high-speed signal path. Indeed, wire bonding a separate PD to the CMOS chip adds additional inductance. This increased inductance is beneficial in isolating the PD junction capacitance from the input of the TIA, but it can also cause undesirable signal peaking if the length of the wire bond is not optimized and controlled, a task difficult to achieve. Consequently, this peaking may result in an incorrect decision at the receiver and in an increased BER. Moreover, the bond pad at the input of the CMOS TIA adds extra capacitance to that node. This increased capacitance limits the bandwidth of the TIA and causes a degradation in the sensitivity if not carefully accounted for in the design. To account for this added capacitance at the input of the TIA, the gain of the amplifier in the TIA needs to be increased or a smaller feedback resistor needs to be used. This enables lower input impedance and improves the bandwidth. However, the increase in the TIA gain leads to an increase in its power consumption, which is not the case in monolithic integration in InP or SiGe technology. Further, smaller feedback resistor can be used to improve the bandwidth, but this degrades the transimpedance of the TIA.

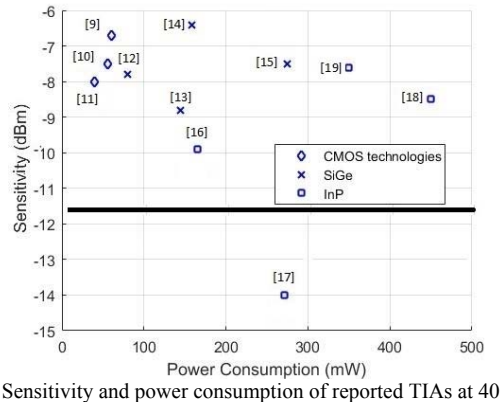

Fig. 2. Sensitivity and power consumption of reported TIAs at 40 Gb/s.

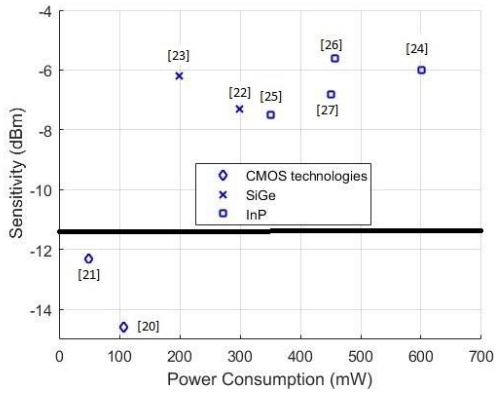

Fig.3. Sensitivity and power consumption of reported TIAs at 50 Gb/s.

The compactness of InP and SiGe monolithically integrated photodetector and TIA chips is an important and attractive feature that is desirable in applications where a small chip size is required for increase bandwidth density. For example, while CMOS TIAs are more compact, the fact that they have to be wire bonded to an external PD, renders the overall design less compact. For example, the PD reported in [28] has a footprint area of 1mm^2 leading to an increased penalty in terms of area. While using flip chip method to connect the PD and the TIA chips results in an overall more compact CMOS system and reduces the parasitic inductance at the input of the TIA, it increases the capacitance due to the proximity of chip pads causing limitations in performance. Hence, InP and SiGe technology provides less complex monolithic approaches with advantage in terms of compactness.

III. Conclusions

We compared the sensitivity and power consumption of TIAs implemented in InP, SiGe, and CMOS at 40 Gb/s and 50 Gb/s. We conclude that CMOS technology outperforms InP and SiGe in terms of power consumption while matching speed and sensitivity. This, however, comes at the cost of a separate photodetector which adds parasitics that can limit the performance of CMOS circuits at higher data rates. The choice of technology for optoelectronics receiver implementation should take into account the power consumption, sensitivity, and compactness of the required final product.

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