BAHAA RADI

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Objective

I am seeking a position in academia as a faculty member or research-driven industry position where I could apply and expand my knowledge in the fields of circuit design and photonics.

Summary

A recent Ph.D. graduate with expertise in:

- Design, simulations, and validation of transistor IC design targeting optical and microwave/RF receivers.
- Embedded systems software and hardware design.
- Antenna design, simulations, and measurements.
- FPGA development.
- PCB design.

Education

Ph.D.: **Electrical and Computer Engineering** Sep 2015-Sep 2020 (expected)
McGill University, Montreal, Canada.

- GPA: 4/4.
- Thesis Title: On the co-design of electronics and photonics for optical communication.
- Advisor: Prof. Odile Liboiron-Ladouceur.
- https://www.mcgill.ca/

MSc: **Microsystems Engineering** Sep 2013-June 2015
Khalifa University (Formerly Masdar Institute), Abu Dhabi, UAE.

- GPA: 4/4.
- Thesis Title: Low power 60GHz transmitter architecture with high Q on-chip resonator/ Low power all-digital phase-locked loop (PLL).
- Advisors: Prof. Ayman Shabra and Prof. Mihai Sanduleanu.
- https://www.ku.ac.ae/

B.Sc.: **Electrical Engineering** Sep 2008 - June 2012
Hashemite University, Zarqa, Jordan.

- GPA: 3.88/4 (Ranked first).
- University Honor List for all years: 2009, 2010, 2011, 2012.
- http://www.hu.edu.jo/

Peer-reviewed journal publications

- **B. Radi**, M. Taherzadeh-Sani, M. S. Nezami, F. Nabki, M. Ménard, and O. Liboiron-Ladouceur, "A 22 Gb/s time-interleaved low-power optical receiver with a two-bit integrating front-end," *IEEE Journal of Solid-State Circuits* (Accepted pending a minor revision, paper ID: JSSC-19-0447.R2).

- **B. Radi**, A. S. Dhillon and O. Liboiron-Ladouceur, "Demonstration of Inter-Chip RF Data Transmission Using On-Chip Antennas in Silicon Photonics," in *IEEE Photonics Technology Letters*, vol. 32, no. 11, pp. 659-662, June 2020, DOI: 10.1109/LPT.2020.2991118.
- **B. Radi**, M. S. Nezami, M. Ménard, F. Nabki, and O. Liboiron-Ladouceur, "A 12.5 Gb/s 1.93 pJ/bit Optical Receiver Exploiting Silicon Photonic Delay Lines for Clock Phases Generation Replacement," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, DOI: 10.1109/TCSII.2019.2952591 (Early access).
- M. S. Nezami, **B. Radi**, M. Taherzadeh-Sani, Y. Xiong, M. Ménard, F. Nabki, and O. Liboiron-Ladouceur, "A High-Speed Moving Average Integrator in Silicon Photonics for TIA-Less Receivers," in IEEE Photonics Technology Letters, vol. 32, no. 17, pp. 1033-1036, Sept 2020, DOI: 10.1109/LPT.2020.3010090.
- M. Taherzadeh-Sani, **B. Radi**, M. S. Nezami, M. Ménard, O. Liboiron-Ladouceur, and F. Nabki, "A 17 Gbps 156 fJ/bit Two-Channel Optical Receiver With Optical-Input Split and Delay in 65 nm CMOS," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 7, pp. 2288-2296, July 2020, DOI: 10.1109/TCSI.2020.2976197.
- M. S. Nezami, **B. Radi**, A. Gour, Y. Xiong, M. Taherzadeh-Sani, M. Ménard, F. Nabki, and O. Liboiron-Ladouceur, "Integrated RF Passive Low-Pass Filters in Silicon Photonics," in *IEEE Photonics Technology Letters*, vol. 30, no. 23, pp. 2052-2055, Dec 2018, DOI: 10.1109/LPT.2018.2875895.

Peer-reviewed conference publications

- **B. Radi**, A. S. Dhillon and O. Liboiron-Ladouceur, "Towards integrated RF photodetector-antenna emitters in silicon photonics," *2020 IEEE Photonics Conference (IPC)* (Accepted for publication, Conference date: September 28th – October 1st, 2020).
- **B. Radi** and O. Liboiron-Ladouceur, "A survey of optical and electronic delay lines with a case study on using optical delay lines in 65nm CMOS optical receivers," in *2020 IEEE International Midwest Symposium on Circuits and Systems(MWSCAS)* (Accepted for publication, Conference date: August 9th – August 12th, 2020).
- **B. Radi**, V. E. Paul, V. Tolstikhin, and O. Liboiron-Ladouceur, "Comparative study of optoelectronics receiver front-end implementation in InP, SiGe, and CMOS," *2016 IEEE Photonics Conference (IPC)*, Waikoloa, HI, 2016, pp. 222-223, DOI: 10.1109/IPCon.2016.7831050.
- H. R. Mojaver, A. Das, **B. Radi**, V. Tolstikhin, K.-W. Leong, and O. Liboiron-Ladouceur, "Scalable SOA-based lossless photonic switch in InP platform," in *Optical Interconnects 2020* (Accepted for publication, Conference date: September 27th – October 1st, 2020).
- V. E. Paul, **B. Radi**, V. Tolstikin, and O. Liboiron-Ladouceur, "A technology-based comparative study for the optoelectronic integration of optical front-ends," *2016 Photonics North (PN)*, Quebec City, QC, 2016, pp. 1-1, DOI: 10.1109/PN.2016.7537902.
- Y. Xiong, F. G. de Magalhães, **B. Radi**, G. Nicolescu, F. Hessel, and O. Liboiron-Ladouceur, "Towards a fast centralized controller for integrated silicon photonic multistage MZI-based switches," *2016 Optical Fiber Communications Conference and Exhibition (OFC)*, Anaheim, CA, 2016, pp. 1-3.
- B. Chalermthai, N. Sada, O. Sarfraz, and **B. Radi**, "Recovery of useful energy from lost human power in gymnasium," *2015 IEEE 15th International Conference on Environment and Electrical Engineering (EEEIC)*, Rome, 2015, pp. 1700-1705, DOI: 10.1109/EEEIC.2015.7165428.

Research and professional experience

Graduate Student Sep 2015-Sep 2020 (expected)
The photonic DataCom team at McGill University, Montreal, Canada.
Projects:

- Novel low power optical receiver design in CMOS 65 nm process technology node.
- Antenna design in the silicon photonics and demonstration of inter-chip data transmission for the first time.
- The design of a photodetector-driven low-pass RC filter and a moving average filter in silicon photonics.

Duties:

- Optical receiver IC design, simulation, layout, tape-out, measurements, and related manuscript drafting. I have fully designed and measured three fully functional receivers in CMOS 65 nm process technology node:
    - A conventional 12.5 Gb/s demultiplex-by-four optical receiver that utilizes optical delay lines for replacing clock phase generation circuits.

- A conventional 17 Gb/s optical demultiplex-by-two improved version of the previous receiver. This receiver achieves an energy efficiency of 156 fJ/bit. This is the best-reported energy efficiency in the literature to date.
- A 22 Gb/s optical receiver with a novel two-bit integrating front-end. This novel front-end allows the receiver to relax the bandwidth requirement of the front-end improving energy efficiency.

The three receivers are complete systems consisting of the analog front-end, the analog-to-digital converter, the decoder, and the output buffers. All three receivers were published in prestigious peer-reviewed journals, as shown in the publications section.

- The design of an on-chip antenna the silicon photonics technology process. This included HFSS simulations, tape-out, measurements of the antenna, and the preparation of the manuscript. For the first time, inter-chip RF data transmission was demonstrated in the silicon photonics platform. This antenna was published in a prestigious peer-reviewed journal, as shown in the publications section.
- The design of a low-pass filter that is driven by a photodetector and a novel moving average filter in the silicon photonics platform. This included modelling, simulations, measurements, and manuscripts preparation. Both filters were published in prestigious peer-reviewed journals, as shown in the publications section.
- The development of an interposer to efficiently package electronics and photonics chips.
- The development of an interface that allows an FPGA with digital outputs to control analog voltage-controlled optical switch matrix. This is done to enable the development of optical switch matrices with a centralized controller.
- Measurements of various optical and electronic systems. I have expertise in using high-end, high-speed measurement equipment, including:
  - pulse pattern generator (PPG),
  - bit-error-rate tester (BERT),
  - real-time scopes, sampling-time scopes,
  - digital communication analyzer (DCA),
  - vector network analyzer (VNA), and
  - RF synthesizers, among other equipment.

Research Assistant at Masdar Institute of Science and Technology. Sep 2013-June 2015
Khalifa University (Formerly Masdar Institute), Abu Dhabi, UAE.
Projects (Semiconductor Research Corporation (SRC) Funded project):

- Low power 60 GHz transmitter architecture with high Q on-chip resonator.
- Low power all digital Phase Locked Loop (PLL).

These projects were funded by Semiconductor Research Corporation (SRC).

Duties:

- The design of a 60 GHz low-noise amplifier (LNA), a 60 GHz power amplifier (PA), and an on-chip antenna in a 65 nm CMOS process stack.
- The design of PCB antennas.
- The design of an all-digital clock and data recovery (CDR) and phase-locked loop (PLL).
- The design of a resonator-based oscillator for the transmitter side of the system.
- On-off keying OOK mm-wave (60 GHz) transmitter design.
- System-level analysis of the transmitter-receiver system.

R&D Embedded Systems Engineer. Sep 2013-June 2015
Ketab Technologies, Amman, Jordan.
Responsibilities included:

- Schematic design.
- Components selection and bill of material (BoM) generation for PCBs.
- Board layout, including footprint generation, component placement, and routing.
- Embedded firmware design, development, and debugging.
- Development and implementation of a frequency hopping firmware for wireless communication.
- Antenna design, matching, optimization.

- PCB design for wireless system on chip (SoC).

Internship: Trainee Engineer May 2011 – July 2011
Tarasol Telecom, Amman, Jordan.

- Assisted with providing technical support to customers using the voice over IP (VoIP) service provided by the company.

Research Knowledge Highlights

- Custom analog, digital, and high-speed IC design.
- Passive components design in CMOS and silicon photonic technology stacks.
- Embedded firmware design (C and assembly languages).
- Using measurement equipment:
  - PPG.
  - VNA.
  - RF synthesizers.
  - BERT.
  - Scopes (Real-time and sampling time).
  - Arbitrary Signal Generator (AWG).
- Antenna design.
- Verilog and FPGA.
- PCB design.
- Embedded hardware design.

Research-Related Computer Software, CAD tools, HDL, and Programming Languages

- Virtuoso Cadence. Specifically, I am familiar with the following technology nodes:
  - TSMC CMOS 65 nm process technology.
  - Global foundries CMOS 65 nm process technology.
  - IBM CMOS 130 nm process technology.
- HFSS: Used for designing different microwave components for on-chip implementation, including antennas, inductors, and capacitors
- OrCAD: Used for PCB schematic design.
- Allegro PCB Designer: Used for PCB layout design.
- MATLAB: A Computational tool.
- C, Embedded C, C++: Used for firmware development.
- Assembly language: Used for firmware development.
- Verilog: Used for describing circuit implementation for implementation in FPGAs.

Teaching Experience

- TA for the advanced digital signals processing course at Masdar Institute of science and technology.
- Conducted four 20-hours introductory training courses to MATLAB in the Jordanian Engineers Association.
- Conducted review sessions for several undergraduate courses, including circuits courses, electronics courses, and signals and systems courses at The Hashemite University.
- Worked as a tutor at A+ Academy in Jordan for different courses related to electrical engineering for six months.

Professional Memberships

- IEEE Solid-State Circuits Society.

Honours and Awards

- McGill Engineering Doctoral Awards ($ 96,000 for three years).

- Masdar Institute of Science and Technology scholarship, which includes tuition fees (4000 AED per month), accommodation, stipend, laptop, books, and health insurance.
- Scholarship for having the highest GPA during bachelor's study (Included tuition fees).
- I placed on the University honours list in each year of study at the Hashemite University (Highest GPA for all years of study).

Languages

- English: full professional proficiency
- French: upper Intermediate level (B2).
- Arabic: native speaker.

Citizenship and Status in Canada

- A Jordanian citizen.
- My current status in Canada: Student.
    - I am in the process of obtaining an open work permit in the October timeframe and the permanent residency afterward.

References

- Will be furnished upon request.